FEATURES

On-Chip Reference and Sample/Hold
320 mW Typical Power Dissipation, 100 MSPS
SNR=67dB at 100 MSPS
SFDR=74dBc @10MHz -1dBFS Ain, 100 MSPS
SNDR=65dB @10MHz -1dBFS Ain, 100 MSPS
2.0 V_{P-P} Differential Analog Input Range
1.8V Supply Operation
LVDS Outputs
Unsigned Binary Output Format

APPLICATIONS

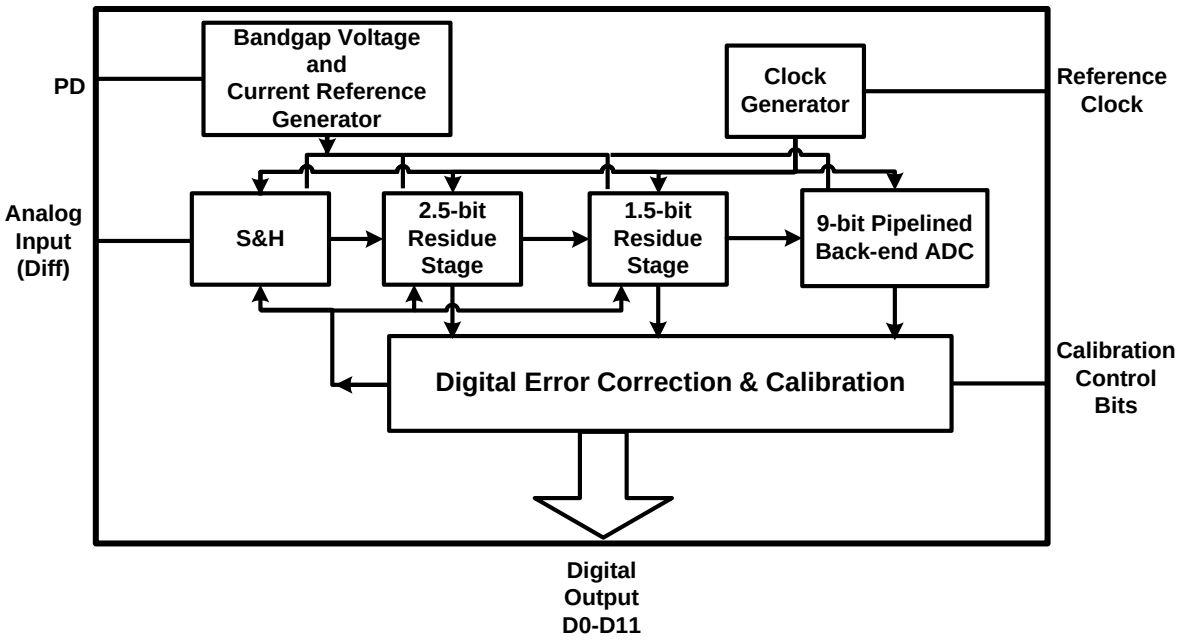
Communications
Base stations and 'Zero-IF' Subsystems
HDTV Broadcast Cameras and Films Scanners

GENERAL INTRODUCTION

The NTAD12100 is a 12-bit monolithic sampling analog-to-digital converter with an on-chip sample-and-hold circuit and is optimized for high-speed conversion and ease of use. The product operates at a 100 MSPS conversion rate with outstanding dynamic performance over its full operating range.

The ADC core requires only a single 1.8V power supply and a 100 MHz sampling clock for full-performance operation. No external reference or driver components are required for many applications. The digital outputs are LVDS compatible. Besides; a 3.3V power supply is needed for ESD protection and I/O pads only. Fabricated on an advanced CMOS process, the NTAD12100 is available in a 64-pin Quad Flat No leads (QFN) package specified over the industrial temperature range (–40˚C to +85˚C).

FUNTIONAL BLOCK DIAGRAM



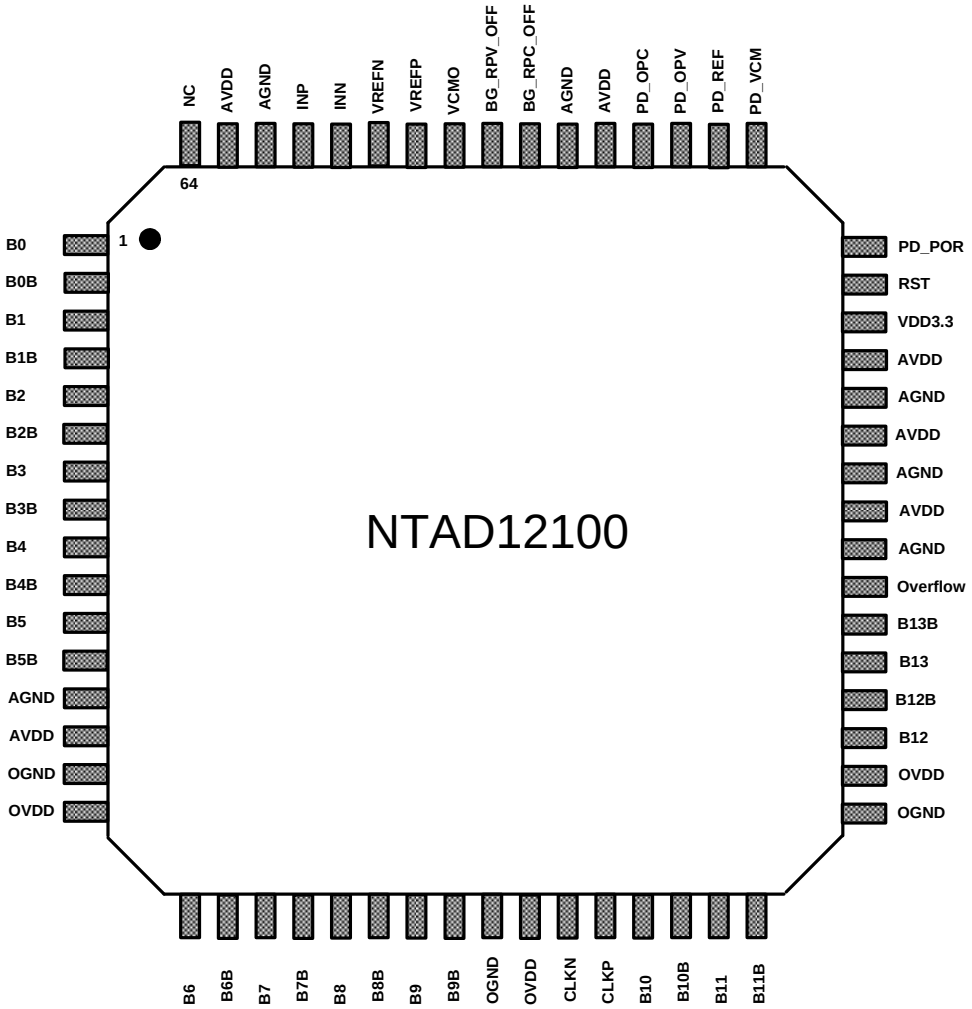
NTAD12100-SPECIFICATIONS

Parameter	Temp	NTAD12100 Min	Typ	Max	Unit
RESOLUTION			12		**Bits**
DC ACCURACY					
Differential Nonlinearity	25°C		±0.4		**LSB**
Integral Nonlinearity	25°C		±1.5		**LSB**
No Missing Codes	25°C		Guaranteed		
Gain Error	25°C		-		**%FS**
ANALOG INPUT					
Input Voltage Range (AIN- $\overline{AIN}$)	25°C		±1		**V**
Common-Mode Voltage	25°C		0.85		**V**
Input Offset Voltage	25°C		-		**mV**
Input Resistance	25°C		2.5		kΩ
Input Capacitance	25°C		4		**pF**
SWITCHING PERFORMANCE					
Maximum Conversion Rate	25°C		100		**MSPS**
Minimum Conversion Rate	25°C		-		**MSPS**
Latency	25°C		5.5		**ns**
DIGITAL INPUTS			3.3V CMOS		
DIGITAL OUTPUTS			LVDS		
Output Coding	25°C		Unsigned Binary		
POWER SUPPLY					
Power Dissipation[1]	25°C		320		**mW**
I_{AVDD}	25°C		114		**mA**
I_{OVDD}	25°C		64		**mA**
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio (SNR) (Without Harmonics) f_{IN}=10MHz	**25°C**		**67**		**dB**
Signal-to-Noise Ratio (SINAD) (With Harmonics) f_{IN}=10MHz	**25°C**		**65**		**dB**
Spurious-Free-Dynamic-Range (SFDR) f_{IN}=10MHz	**25°C**		**74**		**dBc**
Effective Number of Bits f_{IN}=10MHz	**25°C**		**10.5**		**Bits**

[1] Power dissipation measured with a 100MHz sampling clock and a 10MHz sinusoidal analog input.

[2] SNR/harmonics based on an analog input voltage of –0.5 dBFS referenced to a 2 V full-scale input range.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTION



PIN FUNCTION DESCRIPTIONS

Pin Number (NTAD12100)	Mnemonic	Function
1	B0	True Output Bit 0 (LSB)
2	B0B	Complementary Output 0 (LSB)
3	B1	True Output Bit 1
4	B1B	Complementary Output 1
5	B2	True Output Bit 2
6	B2B	Complementary Output 2
7	B3	True Output Bit 3
8	B3B	Complementary Output 3
9	B4	True Output Bit 4
10	B4B	Complementary Output 4
11	B5	True Output Bit 5
12	B5B	Complementary Output 5
13,40,42,44,54,62	AGND	Analog Converter Ground
14, 41,43,45,53,63	AVDD	Analog Supply Voltage. Bypass each pin with a 0.1µF capacitor for best decoupling results (1.8 V).
15,25,33	OGND	Digital Converter Ground. Ground connection for digital circuitry and

		output drivers.
16,26,34	OVDD	Digital Supply Voltage. Bypass with a 0.1µF capacitor for best decoupling results (1.8 V).
17	B6	True Output Bit 6
18	B6B	Complementary Output 6
19	B7	True Output Bit 7
20	B7B	Complementary Output 7
21	B8	True Output Bit 8
22	B8B	Complementary Output 8
23	B9	True Output Bit 9
24	B9B	Complementary Output 9
27	CLKN	Complementary Clock Input. This input ideally requires a $2.2V_{p-p}$ sinusoidal input waveform to maintain the converter's excellent performance.
28	CLKP	True Clock Input. This input ideally requires a $2.2V_{p-p}$ sinusoidal input waveform to maintain the converter's excellent performance.
29	B10	True Output Bit 10
30	B10B	Complementary Output 10
31	B11	True Output Bit 11
32	B11B	Complementary Output 11
35	B12	True Output Bit 12
36	B12B	Complementary Output 12
37	B13	True Output Bit 13 (MSB)
38	B13B	Complementary Output 13 (MSB)
39	Overflow	Output for Out-of-Range Control Bit. If an out-of-range condition is detected, bit "Overflow" flags this condition by transitioning high.
46	VDD3.3	I/O Ring Supply (3.3 V)
47	RST	Input for Reset (Active Low)
48	PD_POR	Input for Power-Down of the Power-ON-Reset Circuitries (Active High)
49	PD_VCM	Input for Power-Down of the Internal VCMO Generator Circuitries (Active High)
50	PD_REF	Input for Power-Down of the Internal reference voltage Generator Circuitries (Active High)
51	PD_OPV	Input for Power-Down of the Internal reference voltage Generator of Band-gap (Active High)
52	PD_OPC	Input for Power-Down of the Internal reference current Generator of Band-gap (Active High)
55	BG_RPC_OFF	I/O Terminal for Connecting an Off-Chip Resistor to Band-gap
56	BG_RPV_OFF	I/O Terminal for Connecting an Off-Chip Resistor to Band-gap
57	VCMO	Output Common Mode Voltage (0.85 V)
58	VREFP	Positive Output Reference (1.35 V).
59	VREFN	Negative Output Reference (0.35 V).
60	INN	Negative Analog Input Terminal. Internally self-biased to 0.85V.
61	INP	Positive Analog Input Terminal. Internally self-biased to 0.85V.
64	NC	Not Connected

DEFINITION OF SPECIFICATIONS

Analog Bandwidth (Small Signal)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of CLKP and CLKN and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Clock Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the clock pulse should be left in Logic "1" state to achieve rated performance; pulsewidth low is the minimum time clock pulse should be left in low state. At a given clock rate, these specs define an acceptable clock duty cycle.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of CLKP and CLKN and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise Plus Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

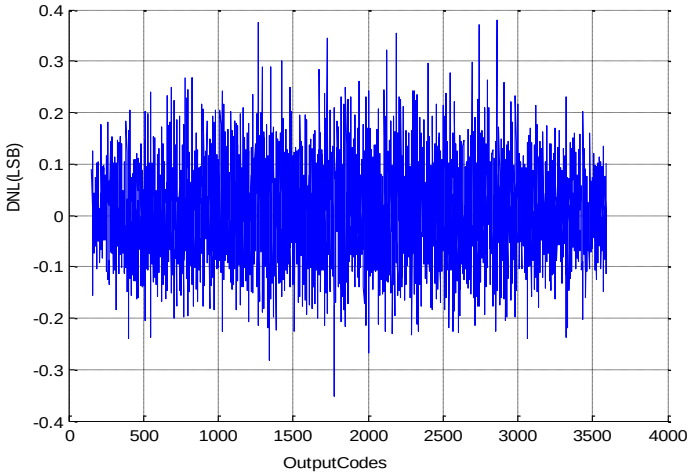
Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

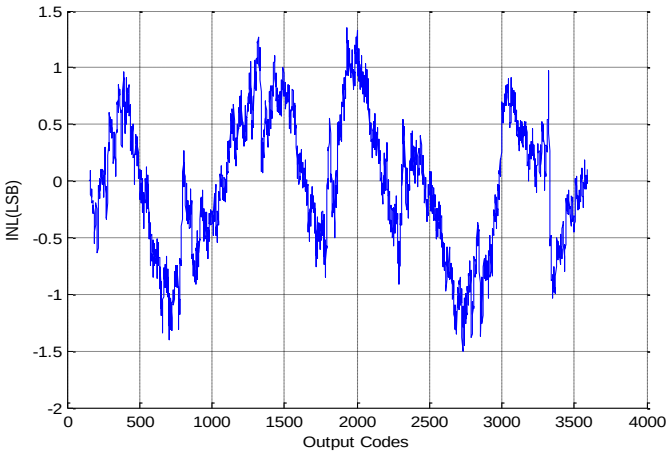
Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Harmonic
The ratio of the rms signal amplitude to the rms value of the worst harmonic component, reported in dBc.

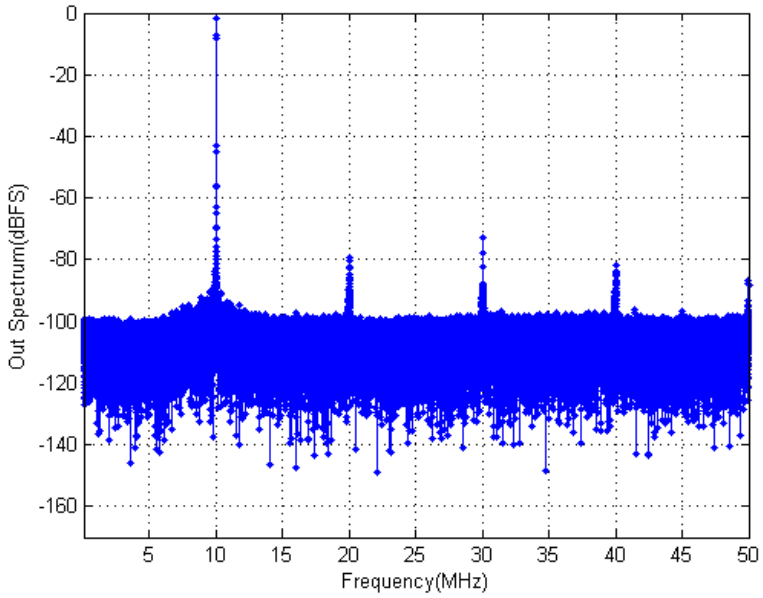
Typical Performance Characteristics–NTAD12100



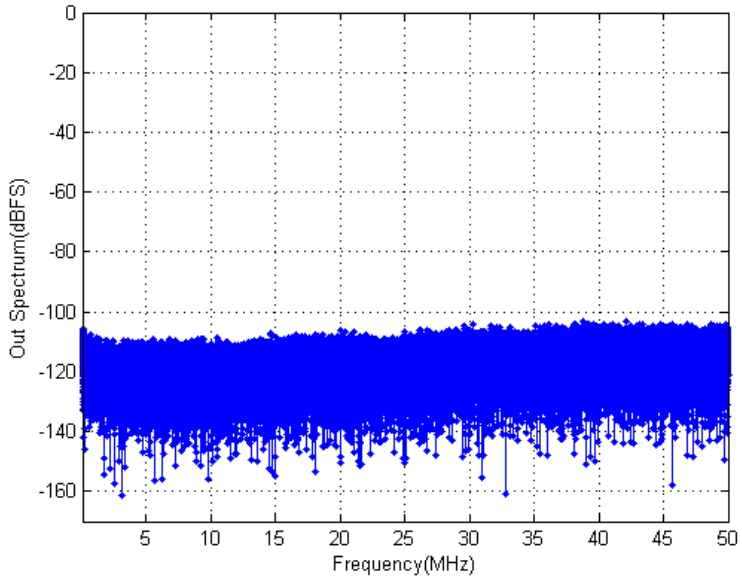
TPC 1. Differential Nonlinearity: f_S = 100 MSPS



TPC 2. Internal Nonlinearity: f_S = 100 MSPS



TPC 3. NTAD12100 output spectrum for -1dB input signal, fin=10MHz, fs=100 MSPS



TPC 4. NTAD12100 output spectrum in absence input signal, to measure SNR

TEST METHOD & CONFIGURATIONS

Document References

Document	Relevant Information
NTAD12100 NikTek Semiconductor Datasheet NTAD12100 Evaluation Board User Manual NTDA24 Evaluation Board User Manual Stratix II EP2S60 DSP Development Board Datasheet from Altera	

General Description

The tests are performed in two separate setups according to the different requirements of evaluating DC and AC specifications of NTAD12100. The DC test is performed using the configuration setup shown in the following figure. In this configuration the NTDA24 EVB[1] is serving as a low frequency highly linear input signal generator for the NTAD12100 EVB. The Wenzel 100MHz low phase noise crystal oscillator provides a low jitter clock source for NTAD12100 EVB. The FPGA Board (Stratix II EP2S60 DSP Development Board) programs the NTDA24 EVB with a NikTek Semiconductor programming code. The digital output data from NTAD12100 EVB is captured by means of the FPGA Board in a slave fashion. The captured data is transferred to a PC and evaluated using NikTek Semiconductor analysis codes.

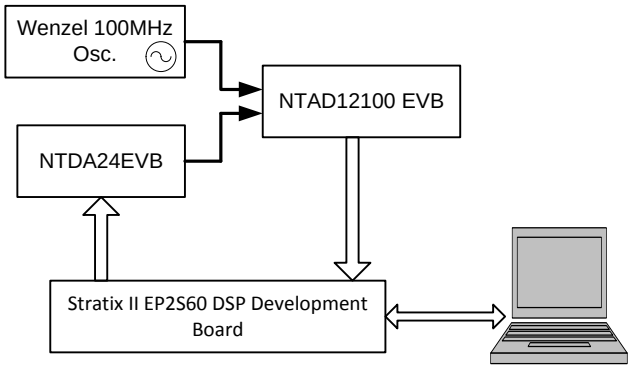


Figure 1. DC test configuration

The next figure shows the appropriate configuration for the AC test. In this configuration the two Wenzel 10MHz and 100MHz low phase noise crystal oscillators provide low jitter sinusoidal input signal and clock source, respectively. The 10MHz input signal passes through the 10MHz Allen Avionic Band-pass filter and drives the NTAD12100 EVB as an input signal. The digital output data from NTAD12100 EVB is captured by means of the FPGA Board in a slave fashion. The captured data is transferred to a PC and evaluated using NikTek Semiconductor analysis codes. It should be mentioned that programming of the FPGA Board and data logging is performed by Altera's Quartus® II software.

[1] Evaluation Board

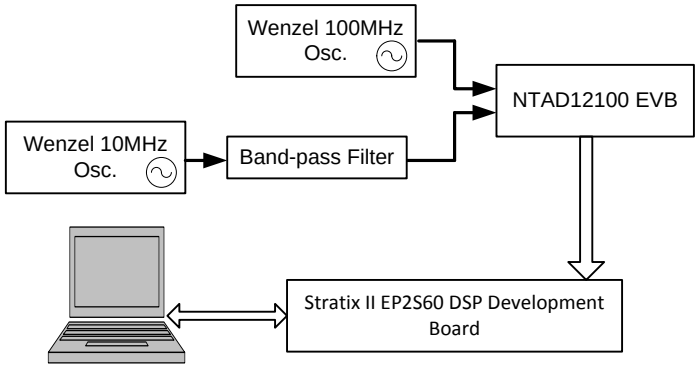


Figure 2. AC test configuration

List of Equipments

Type	Notes
NTAD12100 Evaluation Board	The Main Board
Stratix II EP2S60 DSP Development Board	1) Programming the NTDA24 EVB (DC Test) 2) Capturing the NTAD12100 EVB digital output data (DC & AC Test)
NTDA24 Evaluation Board	Providing a low frequency, highly linear sinusoidal wave form (DC Test)
+5V & ±15V Rechargeable Batteries	Used as clean power supplies for NTDA24 EVB and NTAD12100 EVB
100Msps Oscilloscope + Multimeter a) Some Single-wire SMA Cables b) 5-wire SMA Cable c) 16-wire SMA Cable d) XLR Cable	Checking the intermediate signals a) Connection between the Wenzel oscillators, band-pass filter and NTAD12100 EVB b) Connecting 5-pin headers from FPGA board to NTDA24 Evaluation board c) Connecting NTAD12100 EVB to FPGA board d) Connecting NTDA24 EVB to NTAD12100 EVB
Wenzel 10MHz crystal oscillator	Input signal source (AC Test)
Wenzel 100MHz crystal oscillator	Input clock source (DC & AC Test)
Allen Avionic Band-pass filter	Filtering the input signal source (AC Test)

PCB BOARD DESIGN ISSUES

In order to design the PCB board, the schematic of figure 3 is realized. In this schematic JP4 and JP5 provide the connection ports for an external power supply. The external supply voltage should be between 4.5 to 5 volts. The IC component of U3 is a voltage regulator which generates the regulated 1.8V and 3.3V voltages. Then the regulated 1.8V voltage is passed through three LC filters, providing three ac isolated 1.8V supply voltages. The regulated 3.3V voltage is also passed through two LC filters, providing two ac isolated 3.3V supply voltages. Correspondingly the LC filters provide five isolated GND. It should be mentioned that the GND's are not isolated at dc frequency. Besides; close to the pins of the supply voltages of the IC components, some 100nF decoupling capacitors are used which are connected between the supply voltages and the corresponding grounds. They regulate the bouncing noise due to the long tracks of vdd and gnd.

In order to convert the single-ended clock waveform and the single-ended input signal waveform to the differential waveforms, two transformers are employed (T1 and T2 respectively). The single-ended clock and signal waveforms are generated by low phase noise crystal oscillators of Wenzel Company. The connection between the Wenzel crystal oscillators and the evaluation board is done by two SMA Cables. The equivalent termination load of the oscillators must be 50Ohm. The routing and component placement after the secondary of the above transformers must be done geometrically symmetric. Also it is very important not to insert noisy active components in the path of the clock signal because they induce some phase noise on the clock signal.

The digital outputs of the ADC are connected to the LVDS buffer (U2). The lengths of the related tracks are approximately identical. Then the CMOS outputs of the LVDS buffer are fed to the logic analyzer (FPGA Board) through the connector of JP3. It should be mentioned that the supply and ground voltages of the LVDS buffer are very noisy and they must not be directly connected to the supply and ground voltages of the ADC. In our board design, the isolation is done making use of the LC filters.
In order to achieve an area optimized PCB, the placement of the LVDS buffer is done at the bottom side of the board.

Considering the 100MHz frequency of the board, we have $\frac{\lambda}{4}$=75cm .

The dimension of the board is about 8.5cm×6.5cm . It is considered that the dimension of the board is small enough (Dimension << $\frac{\lambda}{4}$). Therefore there is no transmission line effects and the board can be regarded as a lumped circuit.

It is necessary to provide a capture signal which is fed to the logic analyzer (FPGA board). It triggers the logic analyzer to capture the digital outputs of the ADC, buffered by LVDS buffer, at a proper instance. This is done by employing the T3 transformer, U4 and U5 clock buffers. They provide a CMOS capture signal. The mentioned components don't affect the phase noise characteristics of the clock signal. The bill of material of the required electronic components is shown in the following lists:

The bill of material of the required electronic components

Designator	Component
C1	100nF
C2	100nF
C3	100nF
C4	100nF
C5	100nF
C6	100nF
C7	100nF
C8	100nF
C9	100nF
C10	100nF
C11	100nF
C12	100nF
C13	100nF
C14	100nF
C15	100nF
C16	100nF
C17	100nF
C18	100nF
C19	NC
C20	100nF
C21	100nF
C22	100nF
C23	100nF
C24	100nF
C25	100nF
C26	100nF
C27	100nF
C28	100nF
C29	10uF/16V
C30	220nF
C31	220nF
C32	10uF/16V
C33	10uF/16V
C34	10uF/16V
C35	10uF/16V
C36	10uF/16V
C37	47uF/25V
C38	47uF/25V

C39	47uF/25V
C40	47uF/25V
C41	47uF/25V
C42	47uF/25V
C43	47uF/25V
C44	10pF
C45	100nF
J1	SMA
J2	SMA
J3	CON4
J4	BANANA
J5	BANANA
JP1	HEADER3X2
JP2	HEADER 5X2
JP3	HEADER 20X2
JP4	TP-AGND
JP5	TP-DGND
L1	INDUCTOR1
L2	INDUCTOR1
L3	INDUCTOR1
L4	INDUCTOR1
L5	INDUCTOR1
L6	INDUCTOR1
L7	INDUCTOR1
L8	INDUCTOR1
R1	100
R2	50
R3	50
R4	1M
R5	46K
R6	50
R7	50
R8	50
R9	10K
R10	10K
R11	10K
R12	10K
R13	10k
R14	10k
R15	10k
R16	10k
R17	10k
R18	1k
R19	0
R20	0
R21	33
S1	SW-PB
T1	ADT1-6T
T2	ADT4-1WT
T3	ADT4-1WT
U1	ADC-100MHZ
U2	SN75LVDT386
U3	TPS70351PWP
U4	MPC94551D
U5	MPC94551D

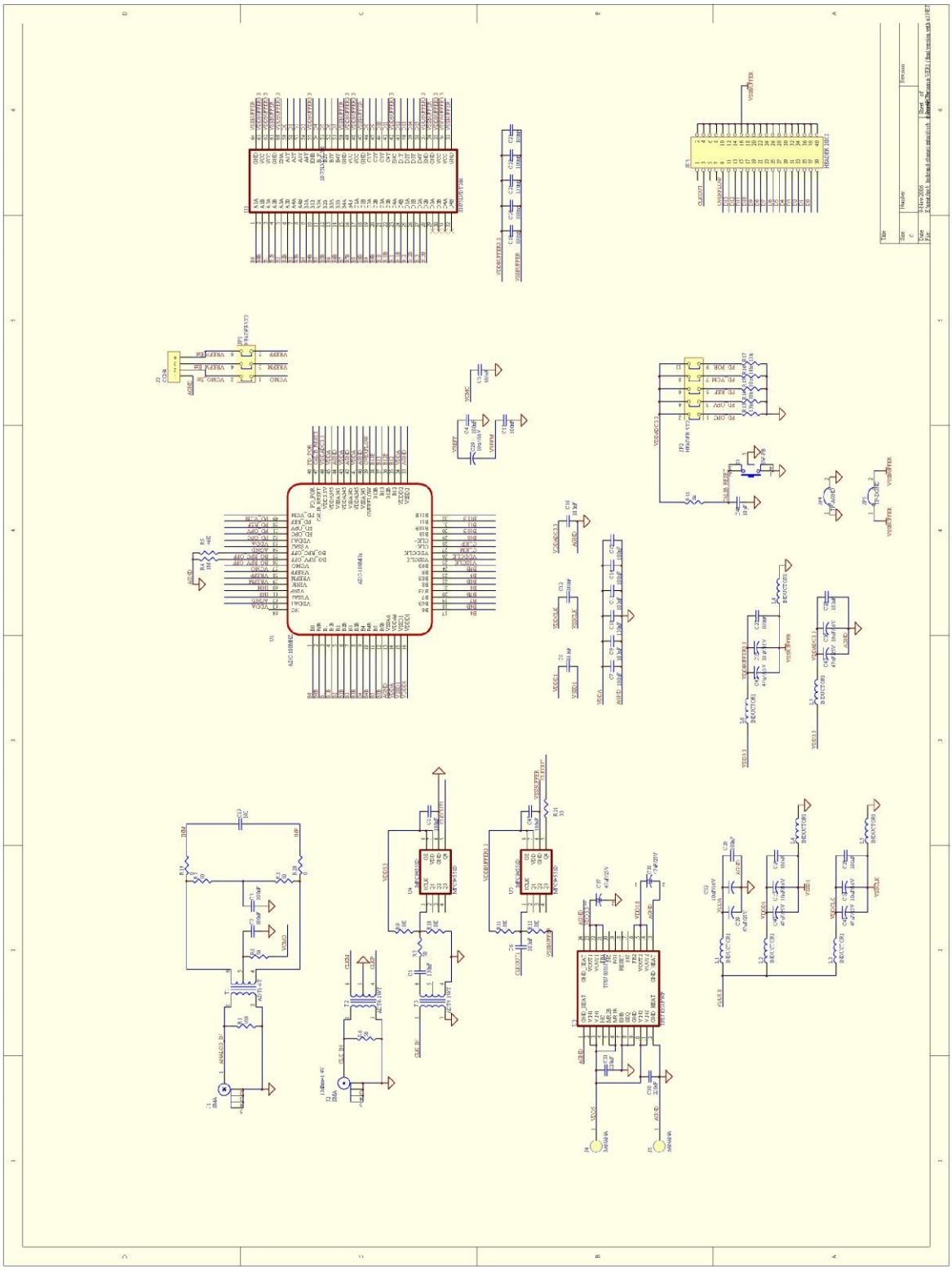


Figure 3. The Schematic of the evaluation board

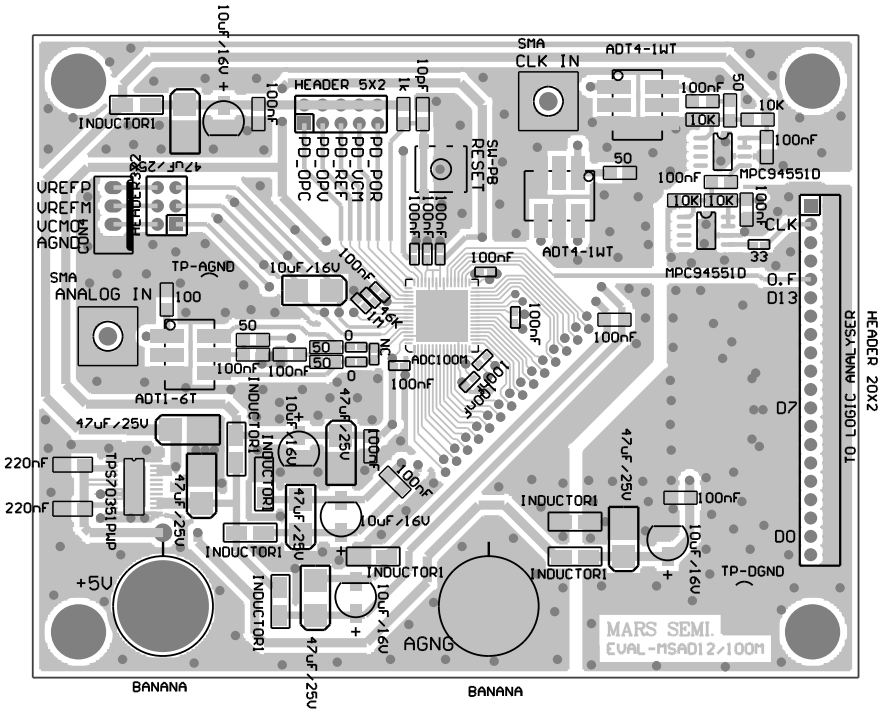


Figure 4. The top side of the PCB

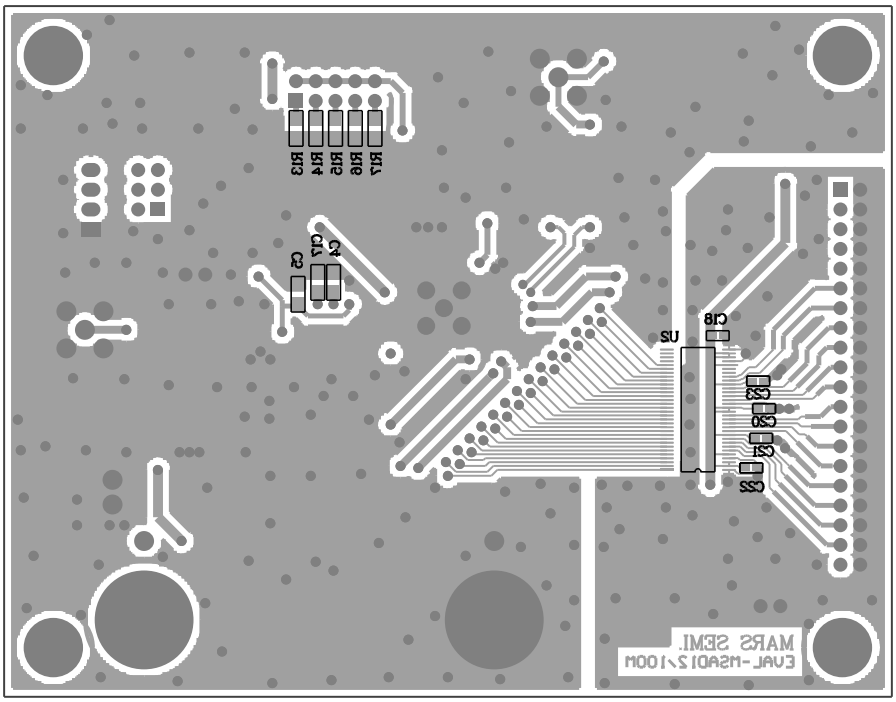


Figure 5. The bottom side of the PCB