FEATURES

3.3 V Mono Audio DAC Systems 1.8 V Digital Interfaces and Circuitry
Multi-Bit Sigma-Delta Architecture
Support 16/20/24-Bit Digital Input Data
Support 48/96/192 kHz Sample Rate
On-Chip Reference Voltage Buffer
Differential Output for Optimum Performance
5.8 V_{p-p} Differential Analog Output Voltage
-97 dB THD+Noise (A-weighted) at 48 kHz
109 dB Dynamic Range at 48 kHz (A-weighted)
37 mW Typical Power Consumption at 48 kHz
On-Chip Volume Control
Digital De-Emphasis Filter for 48/96/192kHz sampling Rate
Support Serial Data Ports Compatible with Right-Justified, Left-Justified, and I^2S
Die Area [mm^2]
Analog Core: 2.7×2
Digital Core: 2.3×2

APPLICATIONS

CD/DVD Audio and Video Players
Home Theater Systems
Portable Consumer Electronics MP3/ Notebook
Sampling Musical Keyboards
Digital Audio Effect Processor

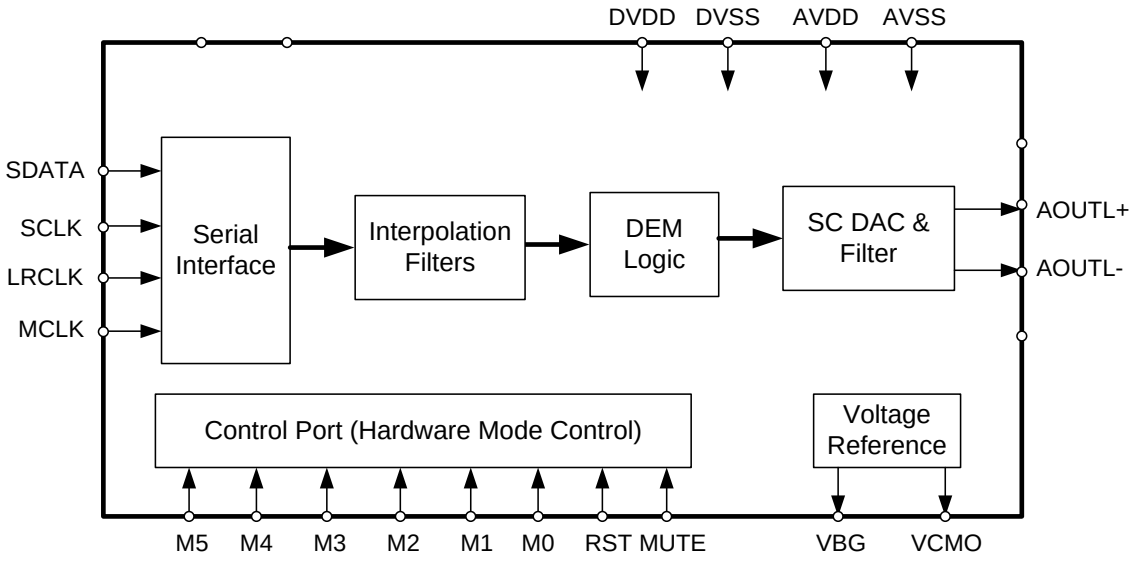
PRODUCT DESCRIPTION

The NTDA24 is a monolithic 24-bit Audio digital-to-analog converter and is optimized for digital audio systems. It accepts PCM as well as direct stream digital (DSD) data at sample rates of 48/96/192 kHz

The NTDA24 is a complete, high performance, single-chip, digital audio playback system. It comprises a high performance digital interpolation filter, a multibit ΔΣ modulator, and a continuous-time voltage-out analog DAC section. Other features include an on-chip mute capability, digital de-emphasis programmed through an SPI compatible serial control port. The NTDA24 operates from a 3.3 V analog power supply with a 1.8 V digital power supply with ±5% power supply tolerances. The NTDA24 is fabricated on a single monolithic integrated circuit and is housed in a 56-lead LQFP package for operating over the temperature range 40°C to +85°C.

Although the DSP is designed for stereo audio, the analog is single channel in this prototype chip.

FUNCTIONAL BLOCK DIAGRAM



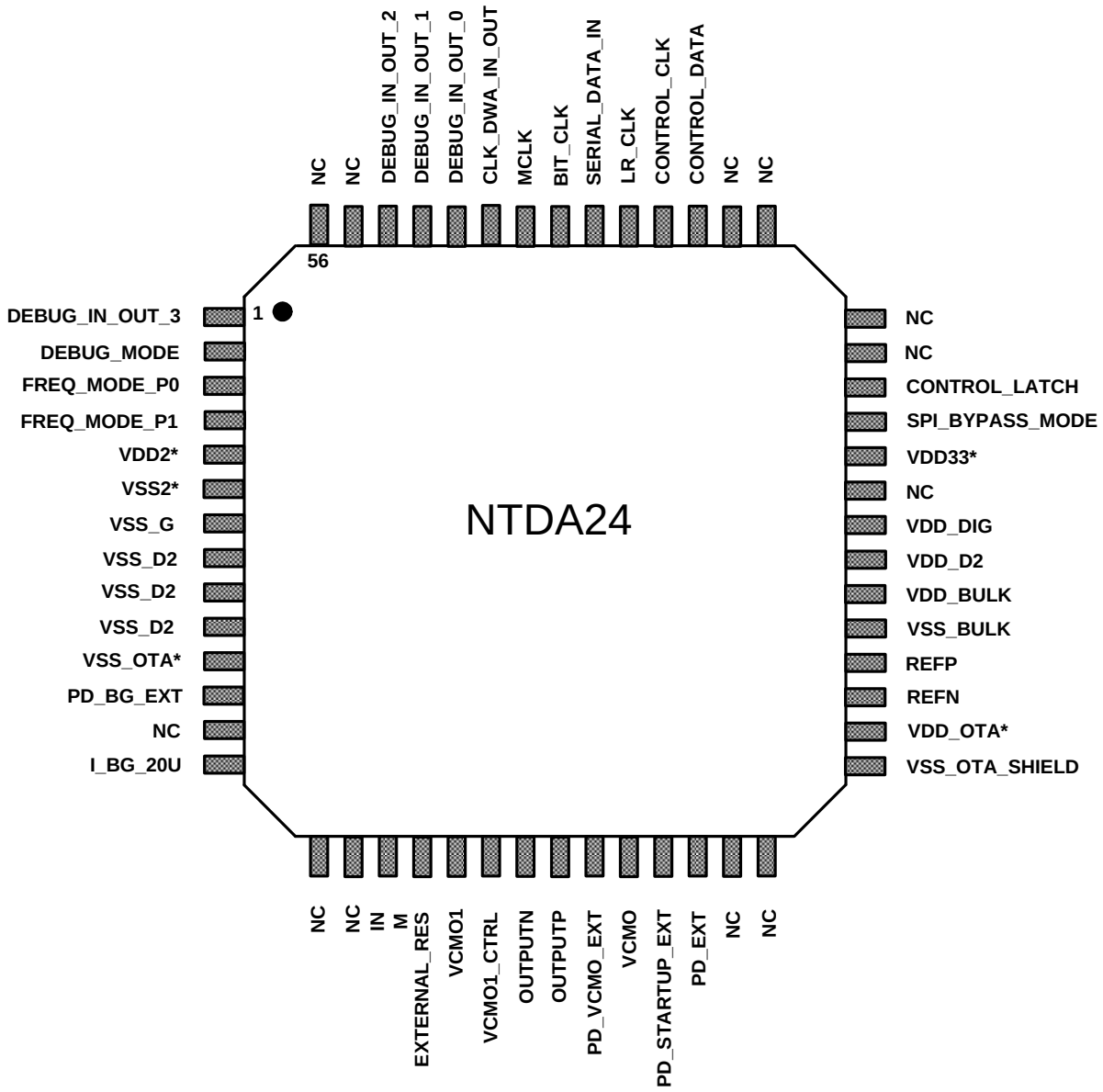
NTDA24-SPECIFICATIONS

TEST CONDITION UNLESS OTHERWISE NOTED

Supply Voltage (AV_{DD}/DV_{DD})	3.3/1.8 V
Ambient Temperature	25°C
Input Clock	12.288 MHz
Input Signal	997 Hz
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 22.5 kHz
Word Length	24 Bits

Parameter	Min	Type	Max	Unit	Test Condition
ANALOG PERFORMANCE					
Dynamic Range (A-Weighted)		109		dB	**20 Hz to 22.5 kHz -60 dBFS**
Total Harmonic Distortion+Noise (A-weighted)		-97		dB	**20 Hz to 22.5 kHz -2 dBFS**
ANALOG OUTPUT					
Full Scale Output Voltage (Differential, p-p)		5.8		Vpp,diff	
Common Mode Voltage		1.5		V	
Output Resistance		1.3		kΩ	
DIGITAL FEATURES					
Volume control step size		0.5		dB	
Volume Control Range(Max Attenuation)		128		dB	
DAC INTERPOLATION FILTER (48 kHz)					
Interpolation Factor		128		-	
Pass Band		20.95		kHz	
Pass-Band ripple		±0.00033		dB	
Stop Band	26.9			kHz	
Stop-Band Attenuation	110			dB	
Group Delay		1005		us	
DAC INTERPOLATION FILTER (92 kHz)					
Interpolation Factor		64		-	
Pass Band		41.9		kHz	
Pass-Band ripple		±0.0002		dB	
Stop Band	53.9			kHz	
Stop-Band Attenuation	110			dB	
Group Delay		500		us	
DAC INTERPOLATION FILTER (192 kHz)					
Interpolation Factor		32		-	
Pass Band		84.2		kHz	
Pass-Band ripple		±0.0002		dB	
Stop Band	107.8			kHz	
Stop-Band Attenuation	110			dB	
Group Delay		250		us	
POWER SUPPLY					
Supply Voltage (Analog)		**3.3**		**V**	
Supply Voltage (Digital1)		**1.8**		**V**	
Supply Voltage (Digital2)		**3.3**		**V**	**Used for ESD Protection**
Supply Current (Analog)		**9.8**		**mA**	
Supply Current (Digital)		**2.5**		**mA**	

PIN CONFIGURATION



	Name	Direction	Description
1	DEBUG_IN_OUT_3	I/O	Debug data in binary mode (used for test of digital/analog parts) ; Digital output (DEBUG=0), Digital input (DEBUG=1)
2	DEBUG_MODE	I	Debug mode (normal=0 , debug mode=1) Debug data is in input mode if debug mode is 1 and Debug data is in output mode if debug mode is 0.
3	FREQ_MODE_P0	I	Frequency mode selection (Table I)
4	FREQ_MODE_P1	I	
5	VDD2*	Power	Positive digital supply (=1.8 V Nominal)
6	VSS2*	Power	Digital ground (=0 V)
7	VSS_G	Power	Digital ground
8	VSS_D2	Power	Ground supply (0V), mixed analog-digital, No.3
9	VSS_D2	Power	Ground supply (0V), mixed analog-digital, No.2

10	VSS_D2	Power	Ground supply (0V), mixed analog-digital, No.1
11	VSS_OTA*	Power	Analog ground (=0 V)
12	PD_BG_EXT	I	Bandgap power down (Normal=0 V, External Bandgap Overwrite= 3.3 V)
13	NC		———
14	I_BG_20U	A/IO	Back-up external bandgap current
15	NC	—	———
16	NC	—	———
17	INM	A/IO	Pin connected to external Resistor R=62.5 KΩ to generate Bandgap current
18	EXTERNAL_RES	A/IO	Pin connected to Pin INM and to the ground by external Resistor R=62.5 KΩ
19	VCMO1	A/I	Current for generating and testing the Vcmo1 voltage externally (=64 µA)
20	VCMO1_CTRL	A/I	Current for generating and testing the Vcmo1 voltage externally (=64 µA)
21	OUTPUTN	A/O	Negative output voltage
22	OUTPUTP	A/O	Negative output voltage
23	PD_VCMO_EXT	I	VCMO power down (Normal=0 V, External VCMO=3.3 V)
24	VCMO	A/IO	Vcmo voltage connected to external capacitor (=Vdd/2)
25	PD_STARTUP_EXT	I	STARTUP power down (Normal=0 V, External STARTUP= 3.3 V)
26	PD_EXT	I	Power down, common between analog and digital parts and also is used for digital system reset (Normal=0 V, power down mode= 3.3 V)
27	NC	—	———
28	NC	—	———
29	VSS_OTA_SHIELD	Power	Analog ground (=0 V)
30	VDD_OTA*	Power	Positive analog supply (=3.3 V Nominal)
31	REFN	Power	Negative reference voltage (=0 V)
32	REFP	Power	Positive reference voltage (=3.3 V Nominal)
33	VSS_BULK	Power	Analog ground (=0 V)
34	VDD_BULK	Power	Positive analog supply (=3.3 V Nominal)
35	VDD_D2	Power	Positive supply (3.3V), mixed analog-digital, No.1
36	VDD_DIG	Power	Positive supply (3.3V), mixed analog-digital, No.2
37	NC		———
38	VDD33*	Power	Positive digital supply (3.3 V)
39	SPI_BYPASS_MODE	I	SPI interface enable (0 enables SPI interface; 1 chooses the control pins instead: 13-14)
40	CONTROL_LATCH	I	Latch input for control data
41	NC	—	———
42	NC	—	———
43	NC	—	———
44	NC	—	———
45	CONTROL_DATA	I	Serial control data MSB first, containing 16 bit of unsigned data
46	CONTROL_CLK	I	Control clock input for control data
47	LR_CLK	I	Left/Right clock input for input data
48	SERIAL_DATA_IN	I	Serial input, MSB first, containing two channels of 16/20/24 bit twos-complement data
49	BIT_CLK	I	Bit clock input for input data
50	MCLK	I	The main input clk (12.288 MHz)
51	CLK_DWA_IN_OUT	I/O	DWACLK is in input mode if debug mode is 1 and in output mode if debug mode is 0.

52	DEBUG_IN_OUT_0	I/O	Debug data in binary mode (used for test of digital/analog parts) ; Digital output (DEBUG=0), Digital input (DEBUG=1)
53	DEBUG_IN_OUT_1	I/O	
54	DEBUG_IN_OUT_2	I/O	
55	NC	—	———
56	NC	—	———

Table I. Mode Selection

FREQ_MODE_P1	FREQ_MODE_P0	Mode Selection
0	0	Single Speed (f_{sIn} = 48 kHz)
0	1	Double Speed (f_{sIn} = 96 kHz)
1	0	Quad Speed (f_{sIn} = 192 kHz)
1	1	Reserved

Table II. Data Format

DF1	DF0	Data Format
0	0	Right-Justified (Default)
0	1	I^2S
1	0	Left-Justified
1	1	Reserved

Table III. Word Width

WL1	WL0	Word Length (No. of Bits)
0	0	24 (Default)
0	1	20
1	0	16
1	1	Reserved

Table IV. De-Emphasis selection

DE_EMP1	DE_EMP0	De-Emphasis Filter
0	0	No Filter
0	1	44.1 kHz Filter
1	0	32 kHz Filter
1	1	48 kHz Filter

Table IV. SPI Control Register

15-13	12	11	10	9	8	6-7	5	4	3	2	1-0
Reserved	PD	DF1	DF0	WL1	WL0	DE-EMP	MUR	MUL	M1	M0	Reg-Select

12	PD	Power-Down Control (1 = Power Down; 0 = Normal Operation (Default))
10-11	DF1-DF0	Data Format (See Table II)
8-9	WL	Word Length Selection (see Table III)
6-7	DE-EMP	De-emphasis selection (see Table IV)
5	MUR	Mute Control Right Channel (0 = Disabled (Default); 1 = Enabled)
4	MUL	Mute Control Left Channel (0 = Disabled (Default); 1 = Enabled)
2-3	M1-M0	Mode Selection (See Table I)
0-1	Reg-Select	00=SPI-Register, 01=left-channel-Volume-control, 10= Right-channel-Volume-control

DEFINITION OF TERMS

Dynamic Range

The ratio of a full-scale input signal to the integrated input noise in the desired bandwidth (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a -60 dB input signal and is equal to (S/[THD+N])+60 dB. Note that spurious harmonics are below the noise with a -60 dB input, so the noise level describes the dynamic range.

Total Harmonic Distortion + Noise

Rms sum of the all spectral components in pass band, excluding the signal power. Expressed in decibles. Measured respect to -8dBFS here.

Pass band

The region of the frequency spectrum unaffected by the attenuation of the digital decimation filter

Pass band Ripple

The peak to peak variation in amplitude response from equal-amplitude input signal frequencies within the pass band, expressed in decibels..

Stop Band

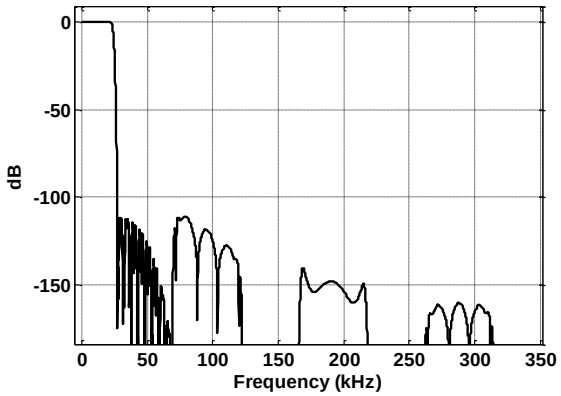
The region of the frequency spectrum attenuated by the digital decimation filter to the degree specified by the stop-band attenuation.

Group Delay

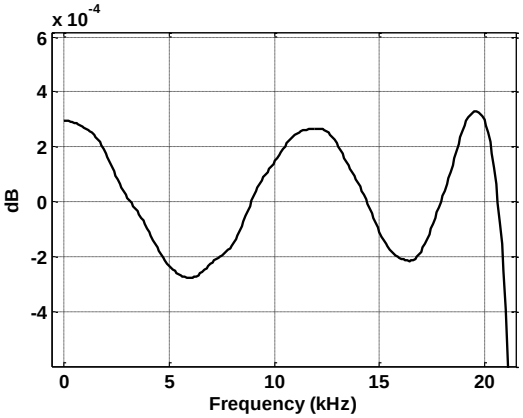
The time interval required for an input pulse to appear ate the converter's output, expressed in millisecond (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

NTDA24-Typical Performance Characteristics

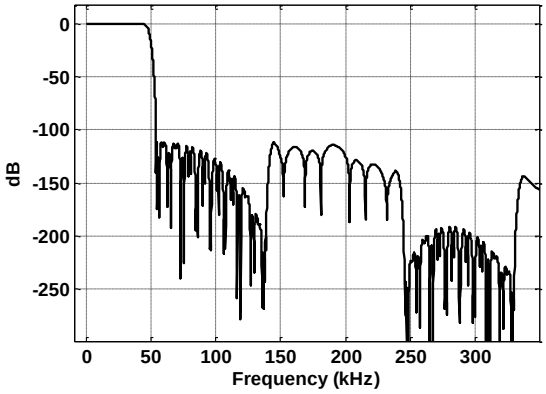
FILTER RESPONSES



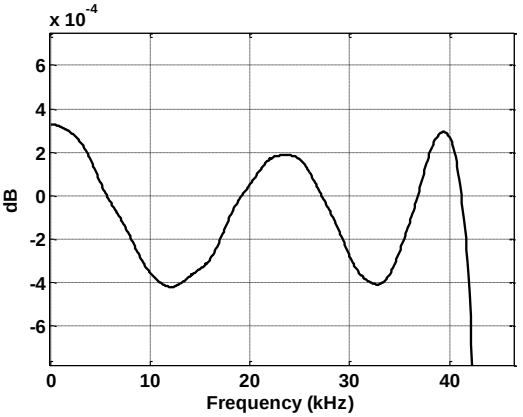
TCP 1. Complete Response, 48 kHz Sample Rate



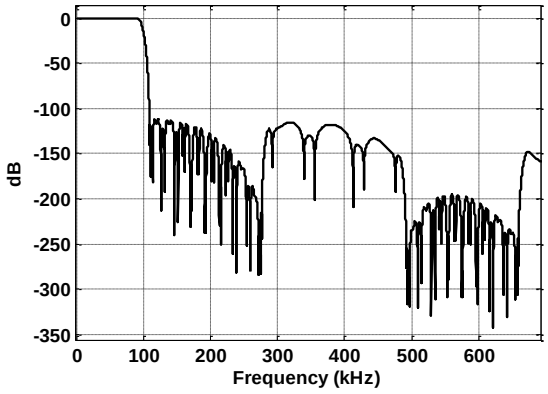
TCP 4. Passband Response, 48 kHz Sample Rate



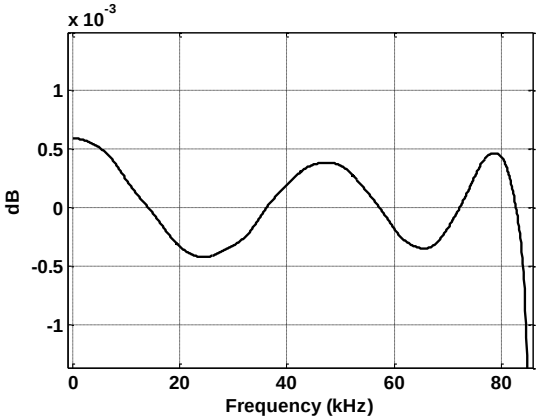
TCP 2. Complete Response, 96 kHz Sample Rate



TCP 5. Passband Response, 96 kHz Sample Rate



TCP 3. Complete Response, 192 kHz Sample Rate



TCP 6. Passband Response, 192 kHz Sample Rate

NTDA24 MEASUREMENTS RESULTS

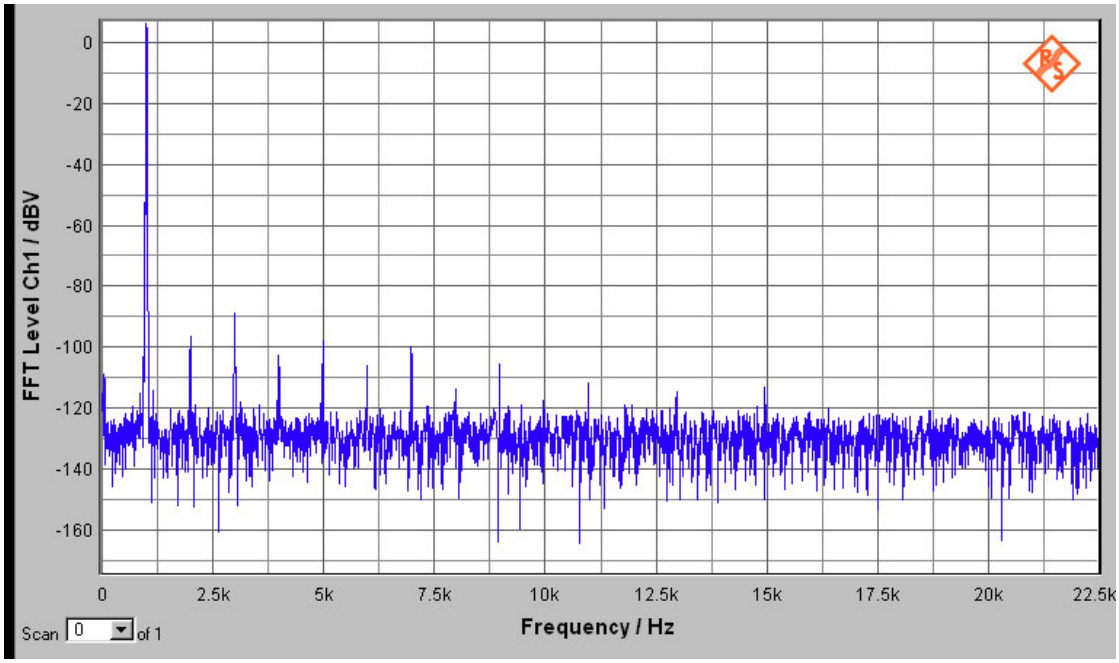


Figure 1. Output spectrum of the NTDA24 evaluation board for 0dBFS input signal and 48kHz sample rate.

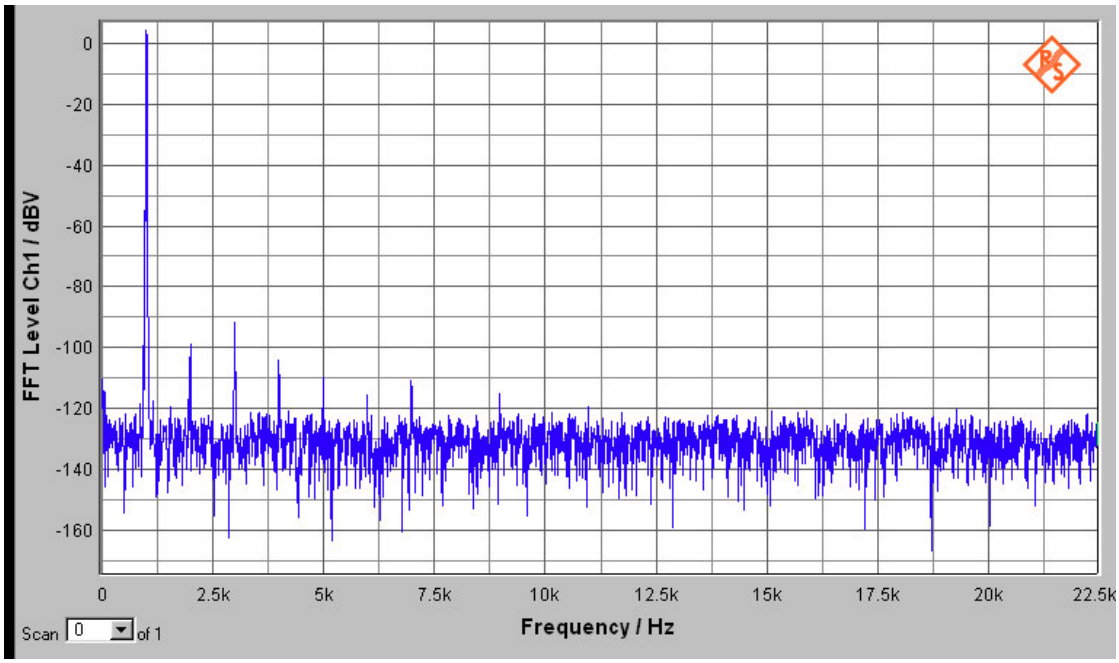


Figure 2. Output spectrum of the NTDA24 evaluation board for -2dBFS input signal and 48kHz sample rate.

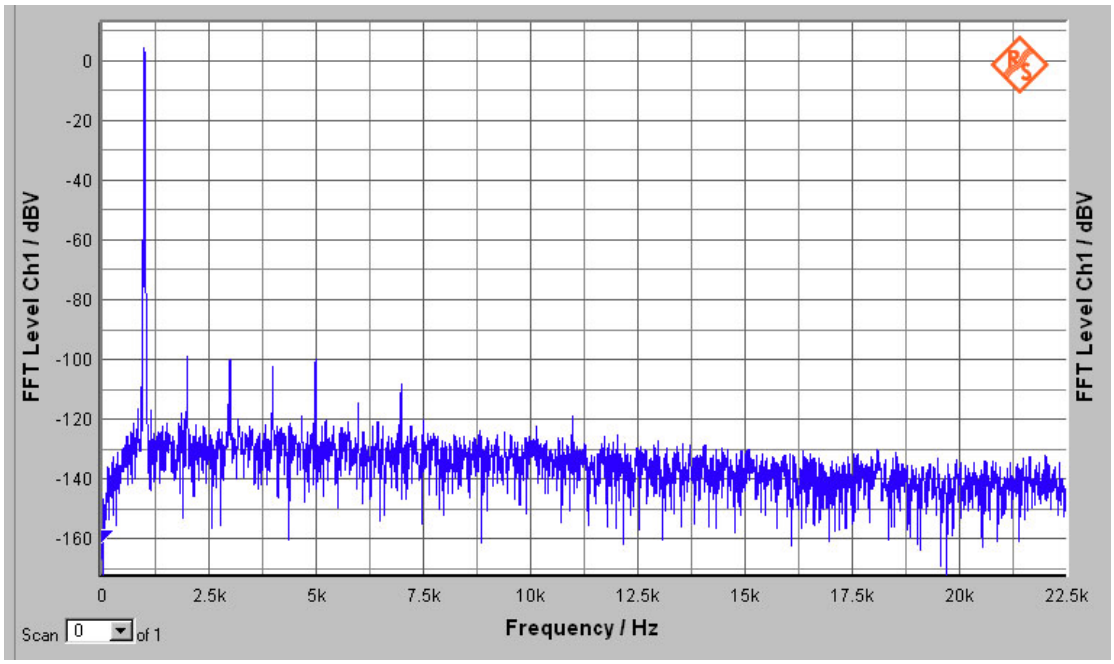


Figure 3. Output spectrum of the NTDA24 evaluation board for -2dBFS input signal and 48kHz sample rate (A-Weighted).

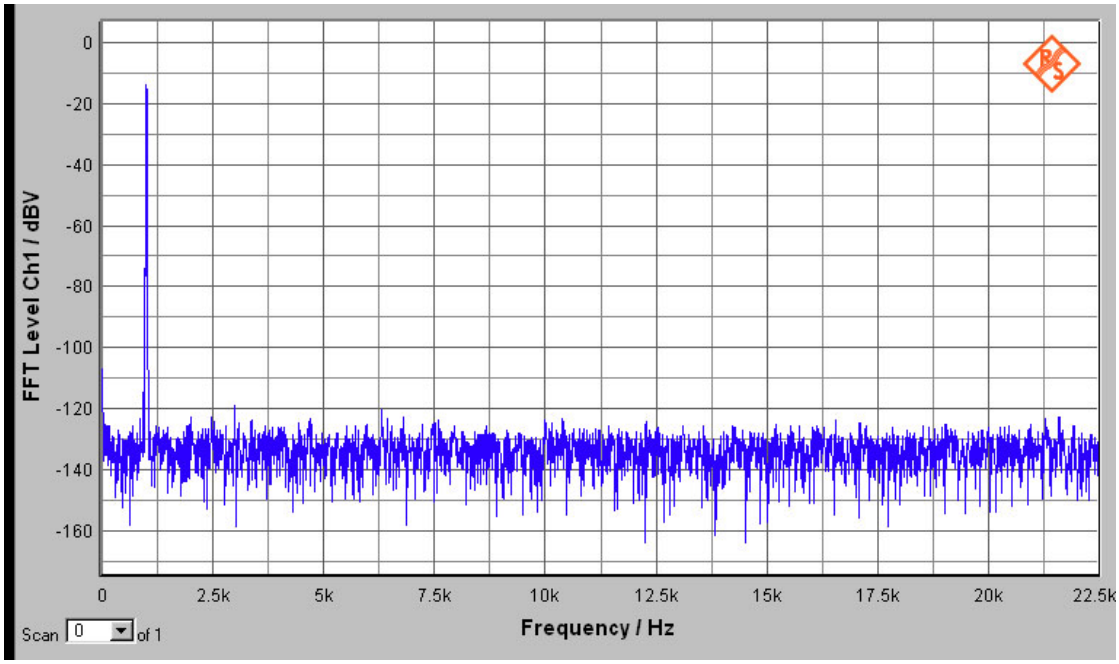


Figure 4. Output spectrum of the NTDA24 evaluation board for -20dBFS input signal and 48kHz sample rate.

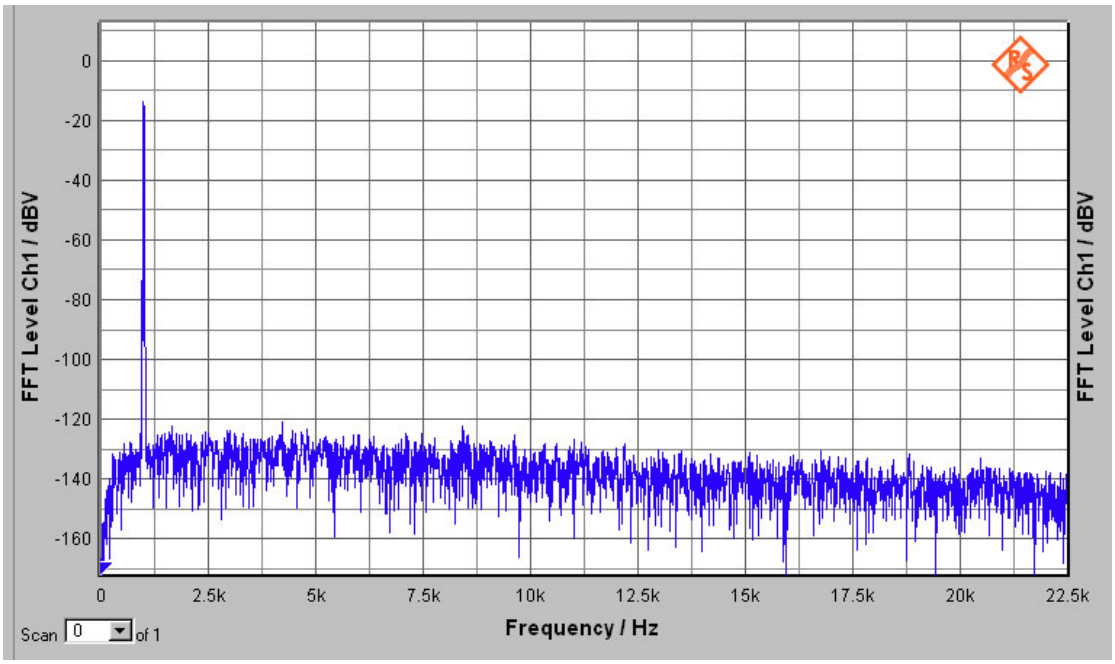


Figure 5. Output spectrum of the NTDA24 evaluation board for -20dBFS input signal and 48kHz sample rate (A-Weighted).

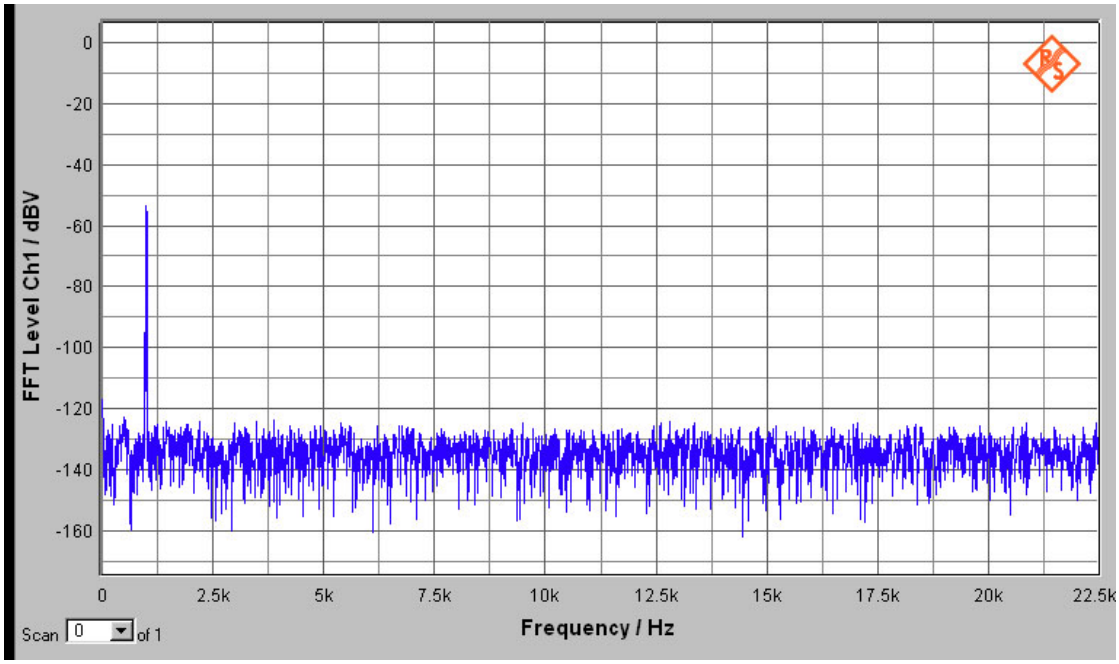


Figure 6. Output spectrum of the NTDA24 evaluation board for -60dBFS input signal and 48kHz sample rate.

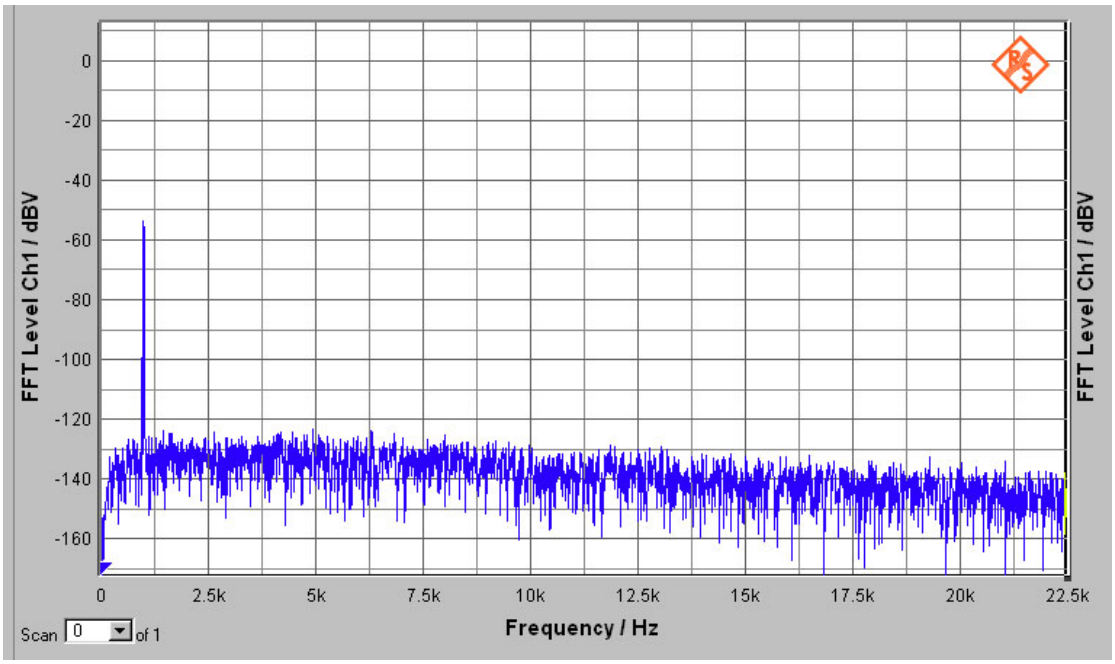


Figure 7. Output spectrum of the NTDA24 evaluation board for -60dBFS input signal and 48kHz sample rate (A-Weighted).

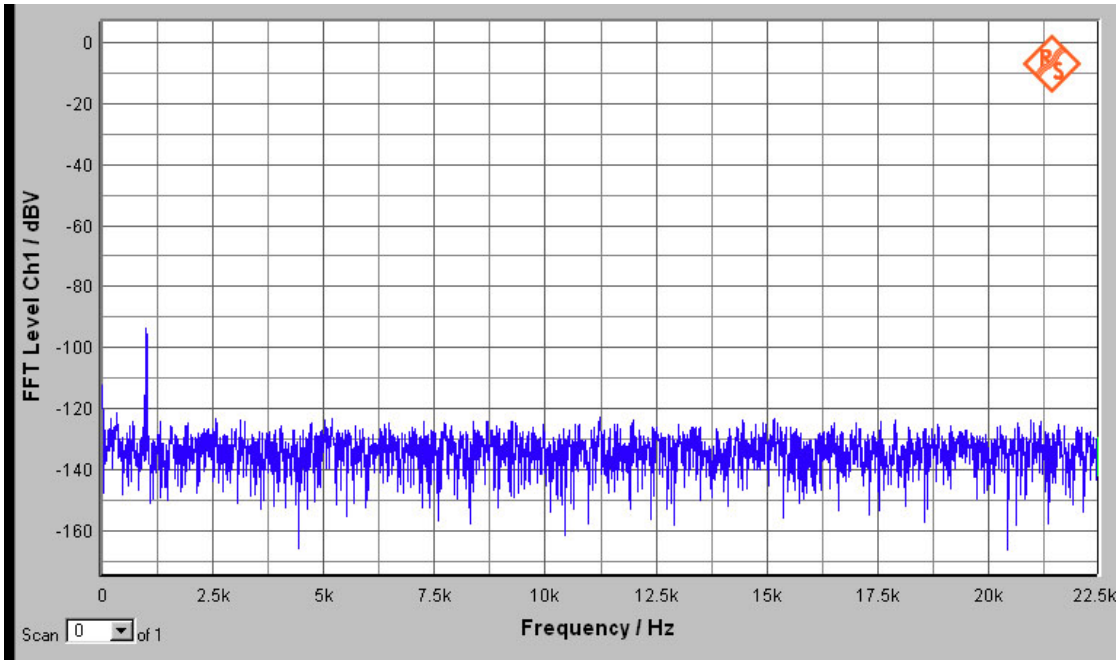


Figure 8. Output spectrum of the NTDA24 evaluation board for -100dBFS input signal and 48kHz sample rate.

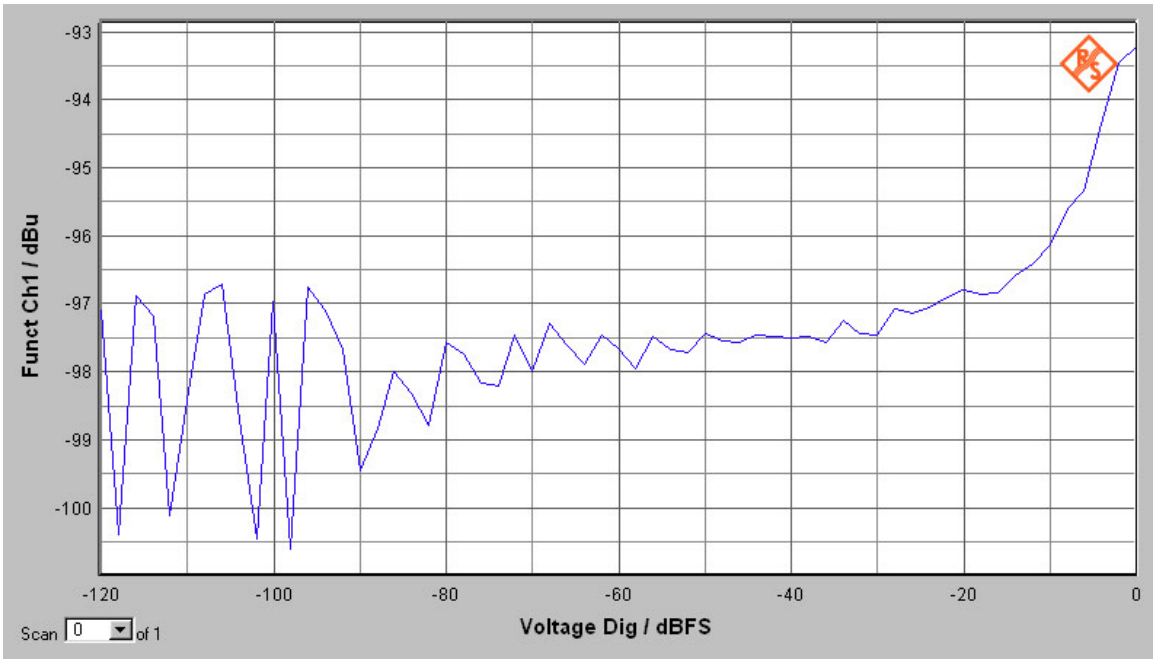


Figure 9. Noise level of the NTDA24 evaluation board versus the power of the input signal and 48kHz sample rate.

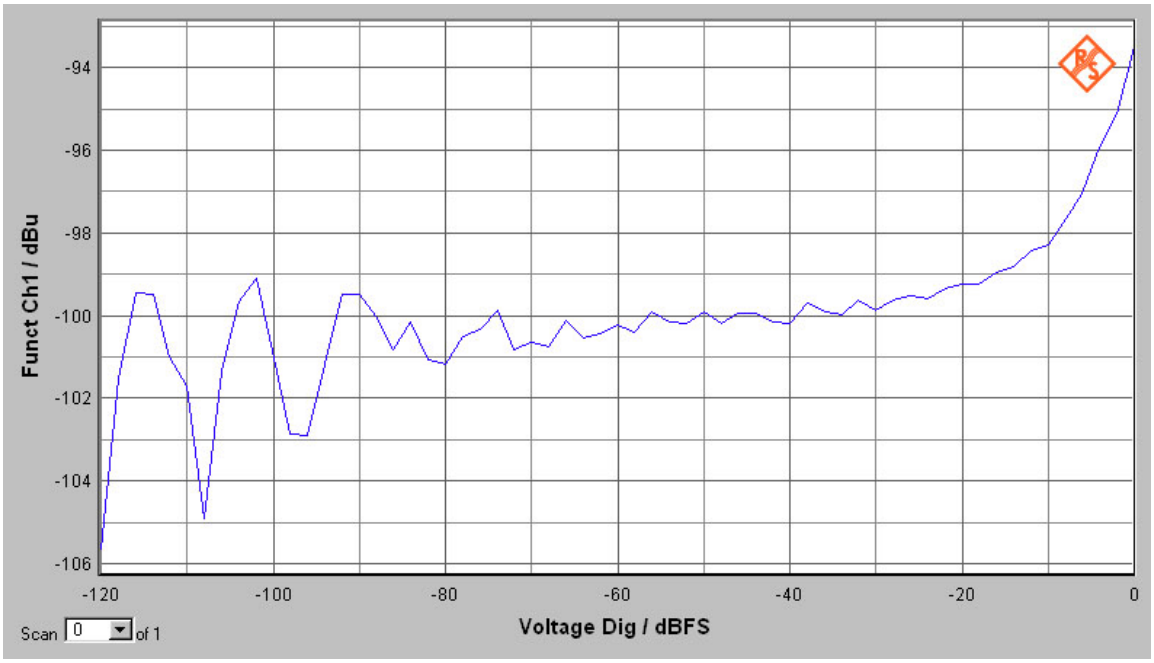


Figure 10. Noise level of the NTDA24 evaluation board versus the power of the input signal and 48kHz sample rate (A-Weighted).

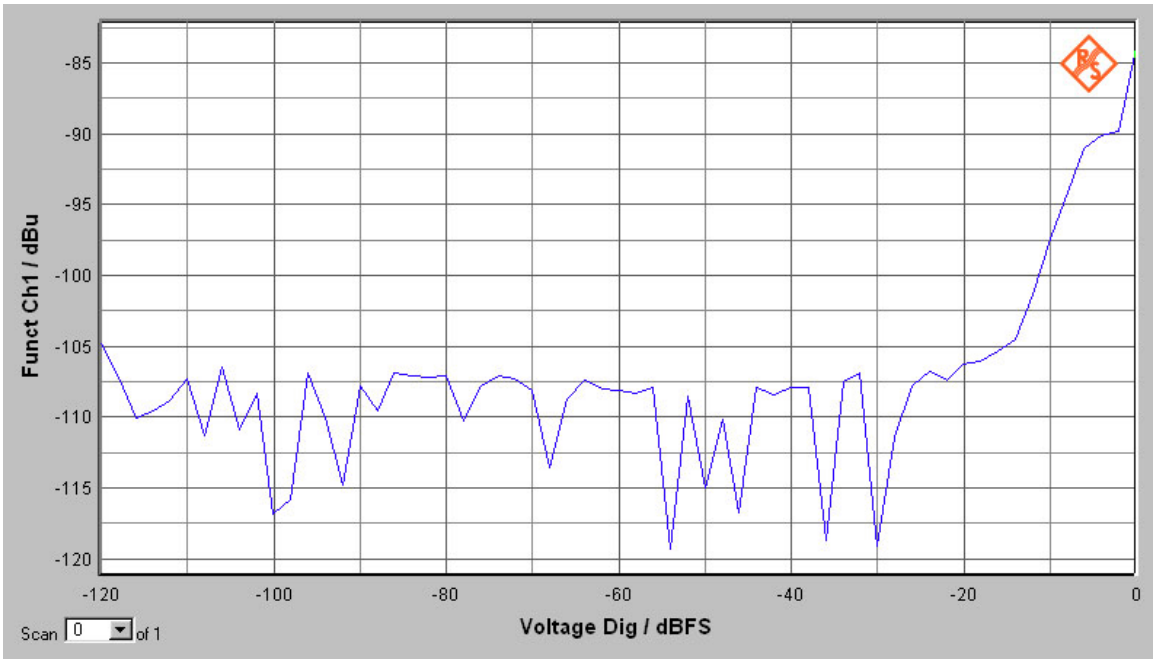


Figure 11. THD level of the NTDA24 evaluation board versus the power of the input signal when sample rate is 48kHz.

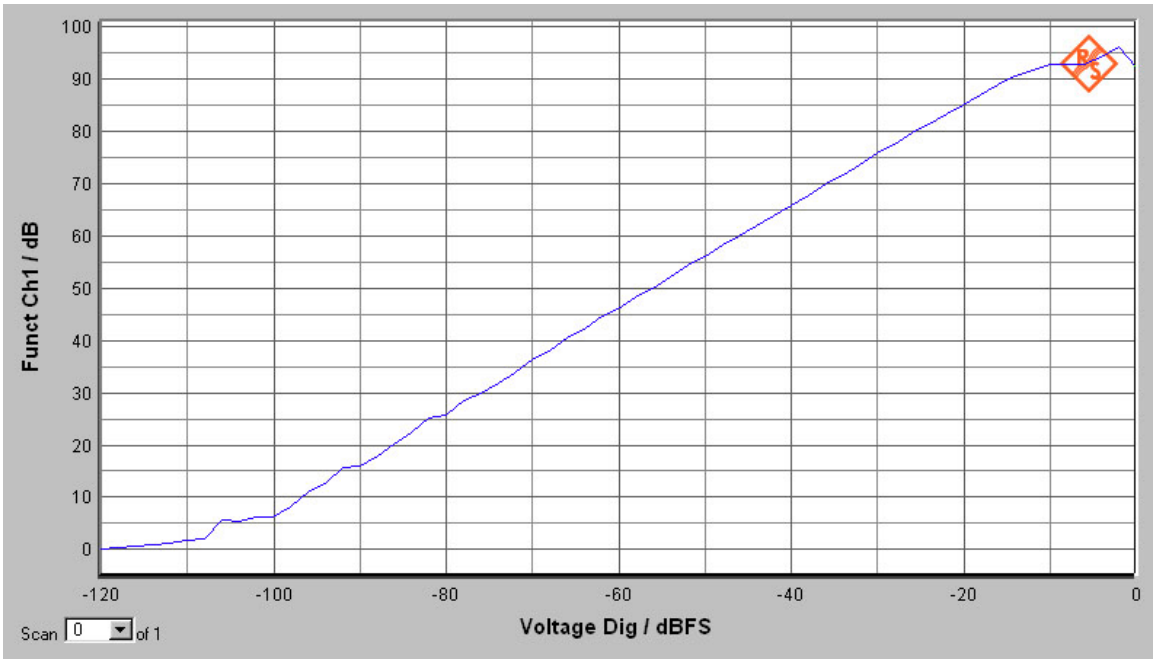


Figure 12. SNDR of the NTDA24 evaluation board versus the power of the input signal when sample rate is 48kHz.

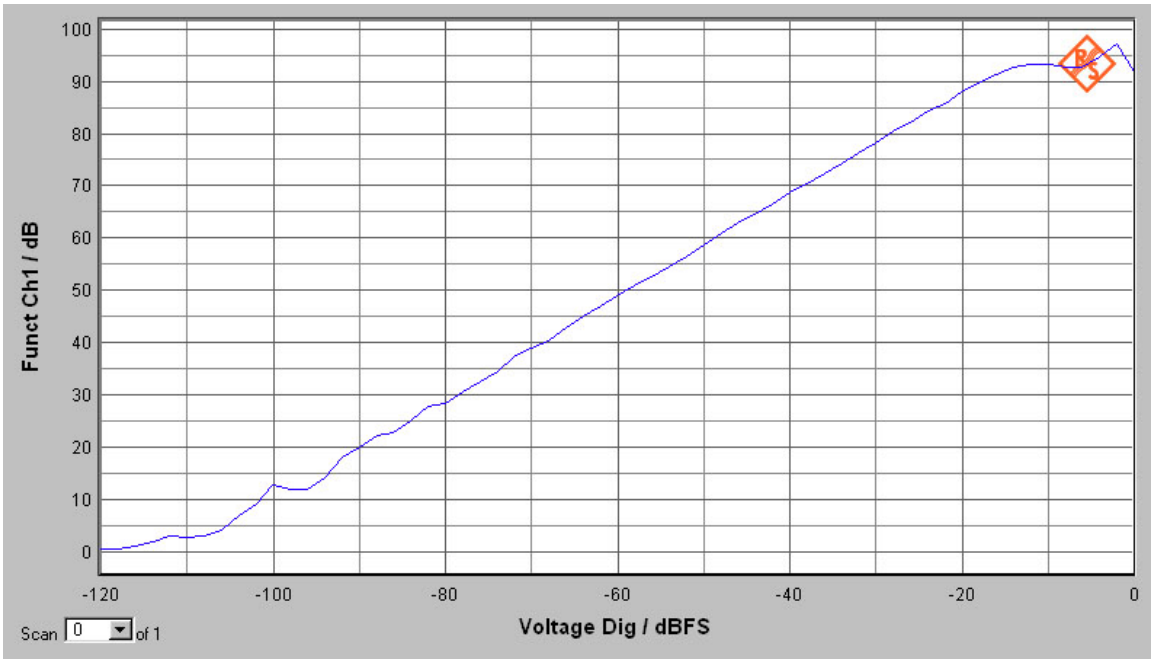


Figure 13. SNDR of the NTDA24 evaluation board versus the power of the input signal when sample rate is 48kHz (A-Weighted).

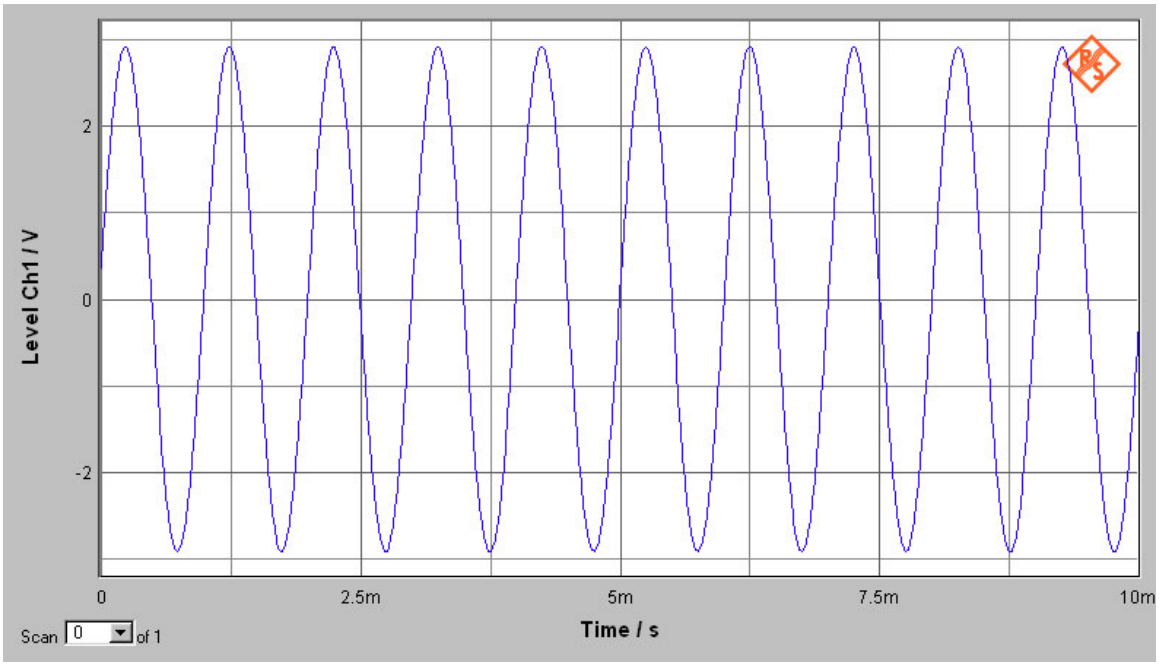


Figure 14. Output signal of the NTDA24 evaluation board in the time domain when the input signal is 0dBFS and sample rate is 48kHz.

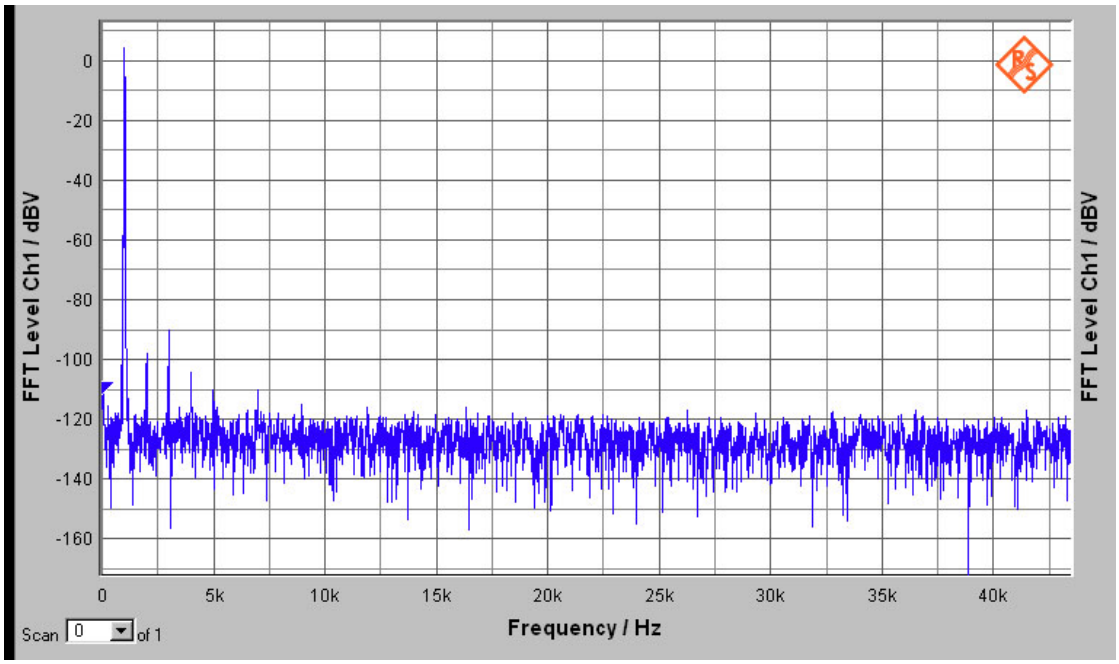


Figure 15. Output spectrum of the NTDA24 evaluation board for -2dBFS input signal and 96kHz sample rate.

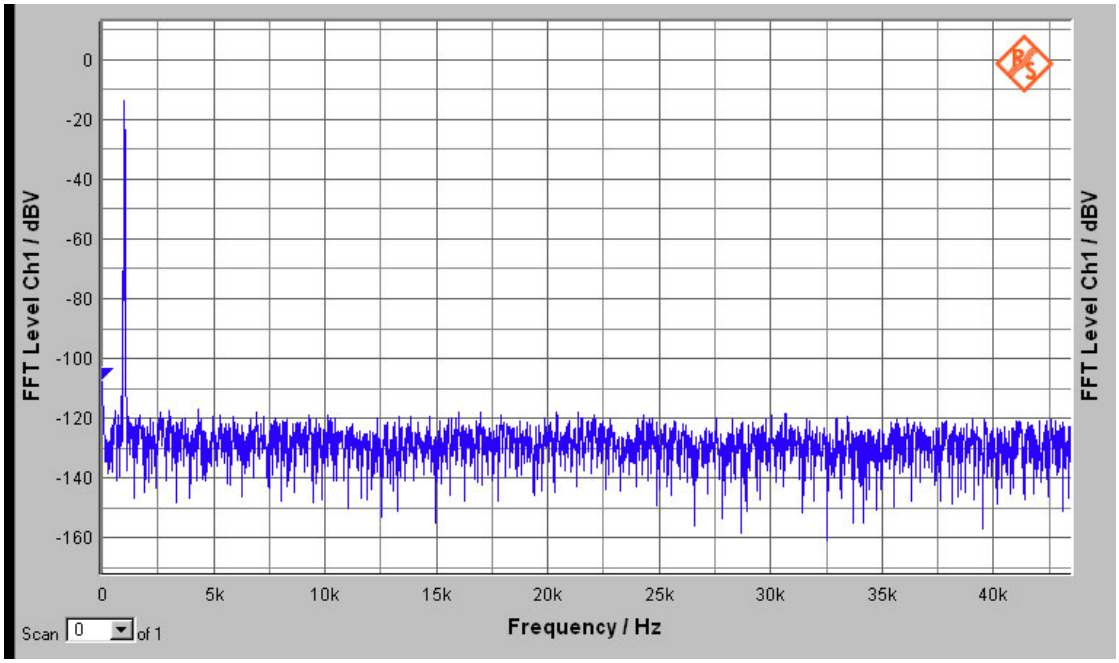


Figure 16. Output spectrum of the NTDA24 evaluation board for -20dBFS input signal and 96kHz sample rate.

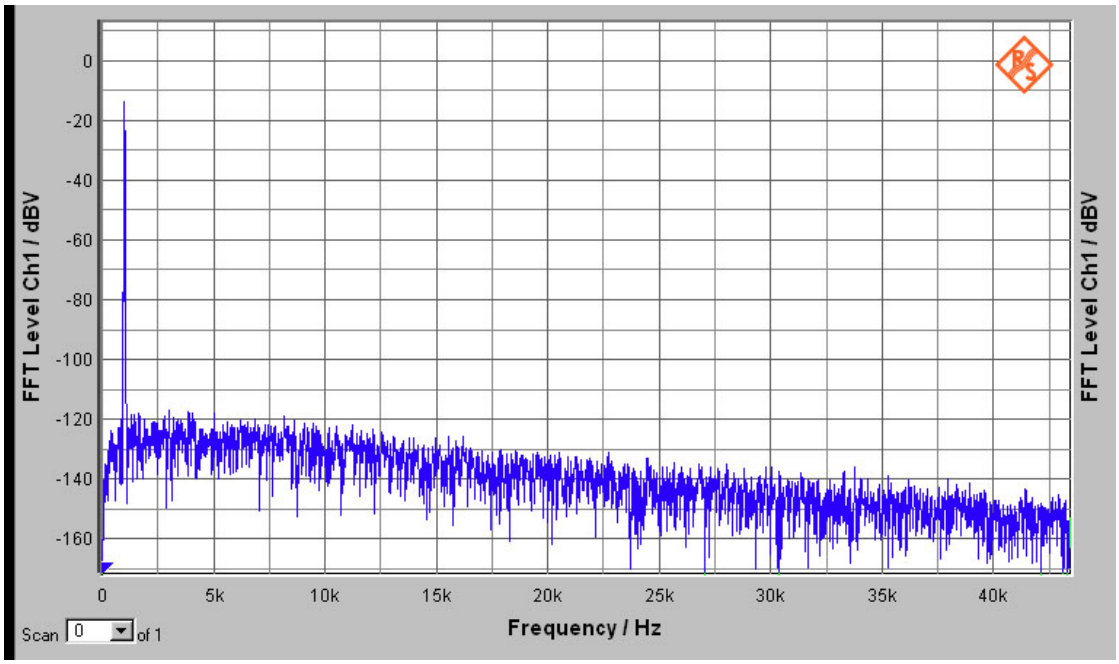


Figure 17. Output spectrum of the NTDA24 evaluation board for -20dBFS input signal and 96kHz sample rate (A-Weighted).

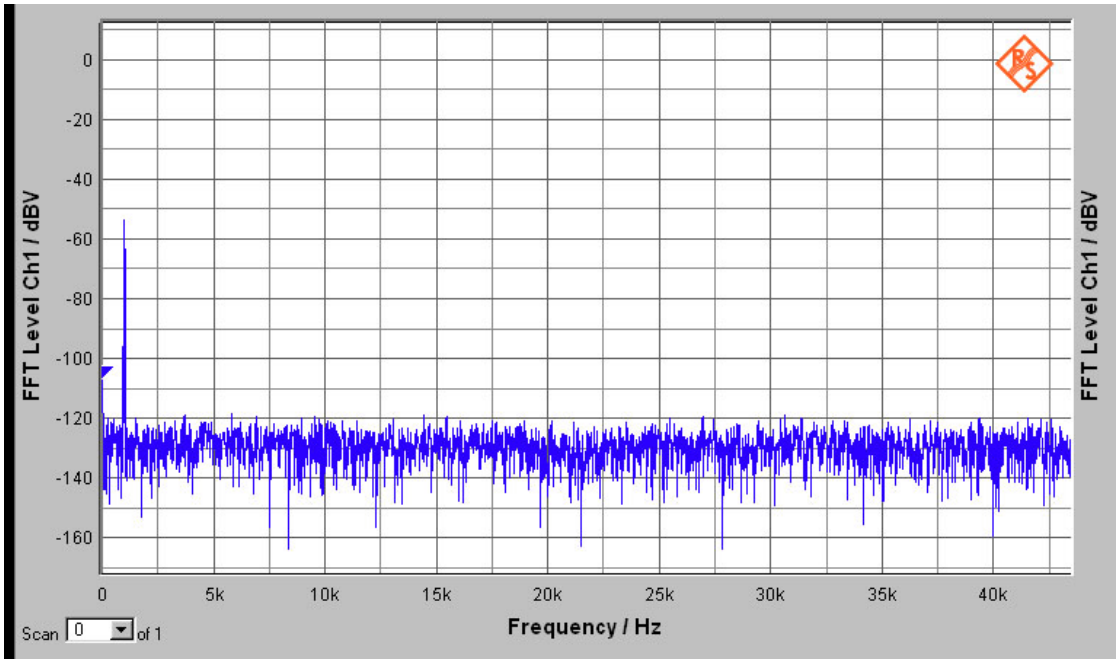


Figure 18. Output spectrum of the NTDA24 evaluation board for -60dBFS input signal and 96kHz sample rate.

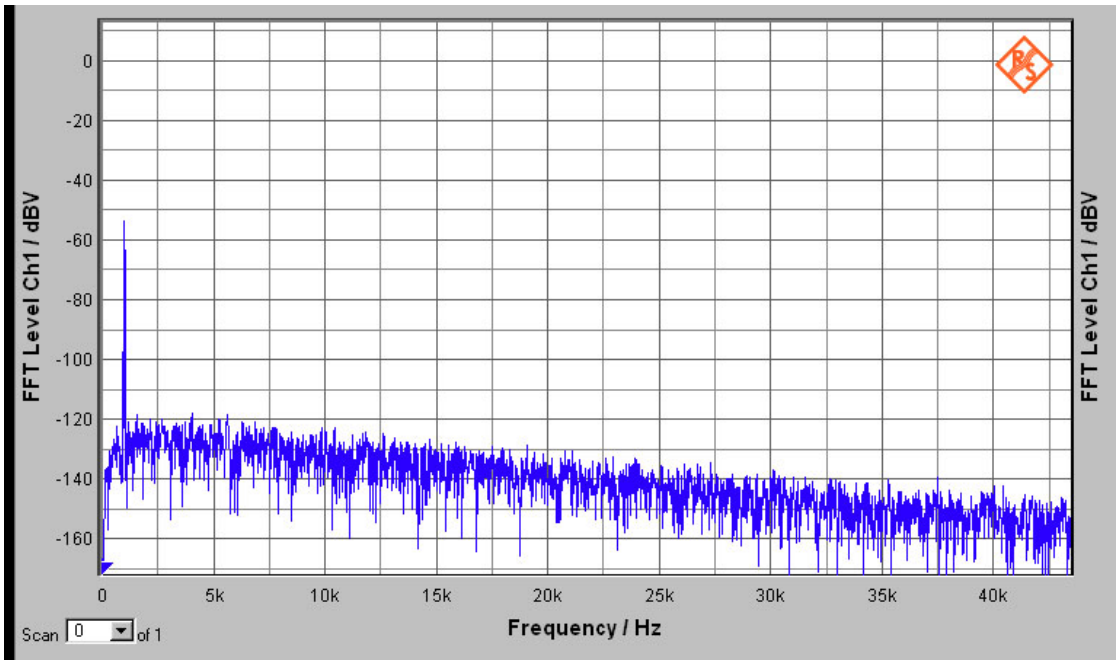


Figure 19. Output spectrum of the NTDA24 evaluation board for -60dBFS input signal and 96kHz sample rate (A-Weighted).

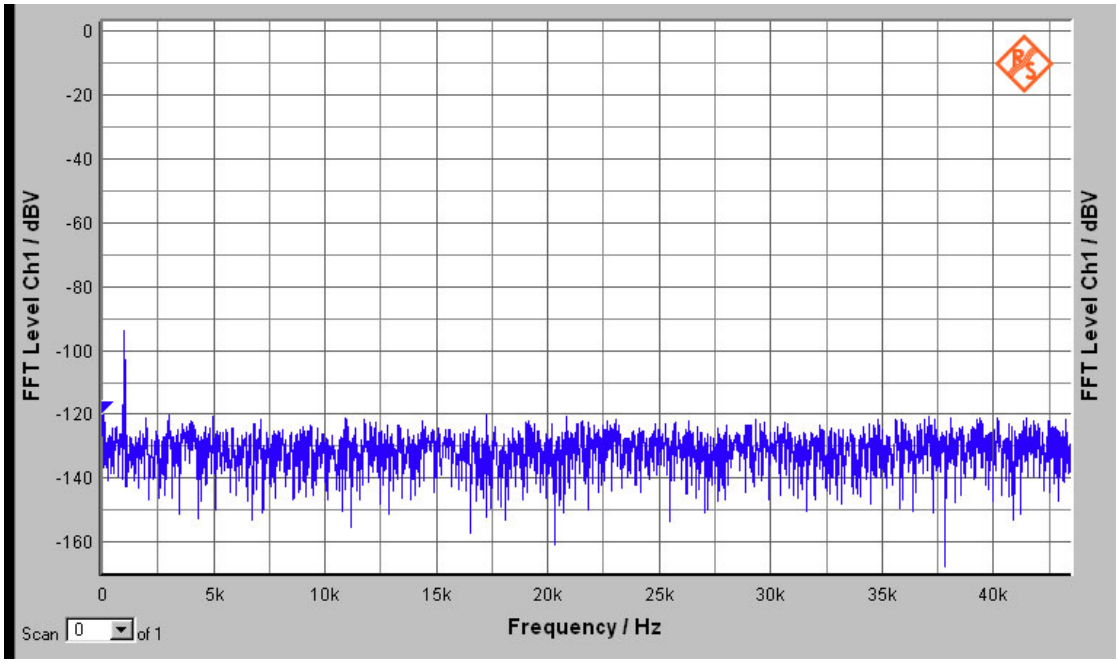


Figure 20. Output spectrum of the NTDA24 evaluation board for -100dBFS input signal and 96kHz sample rate.

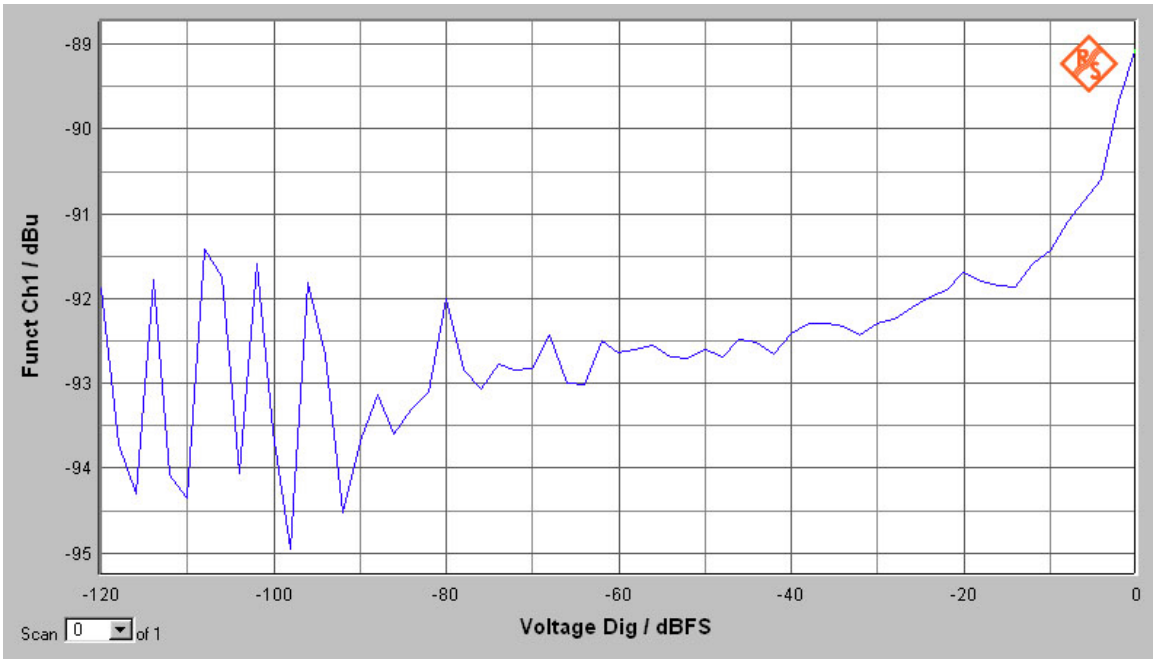


Figure 21. Noise level of the NTDA24 evaluation versus the power of the input signal when sample rate is 96kHz (BW= 46kHz).

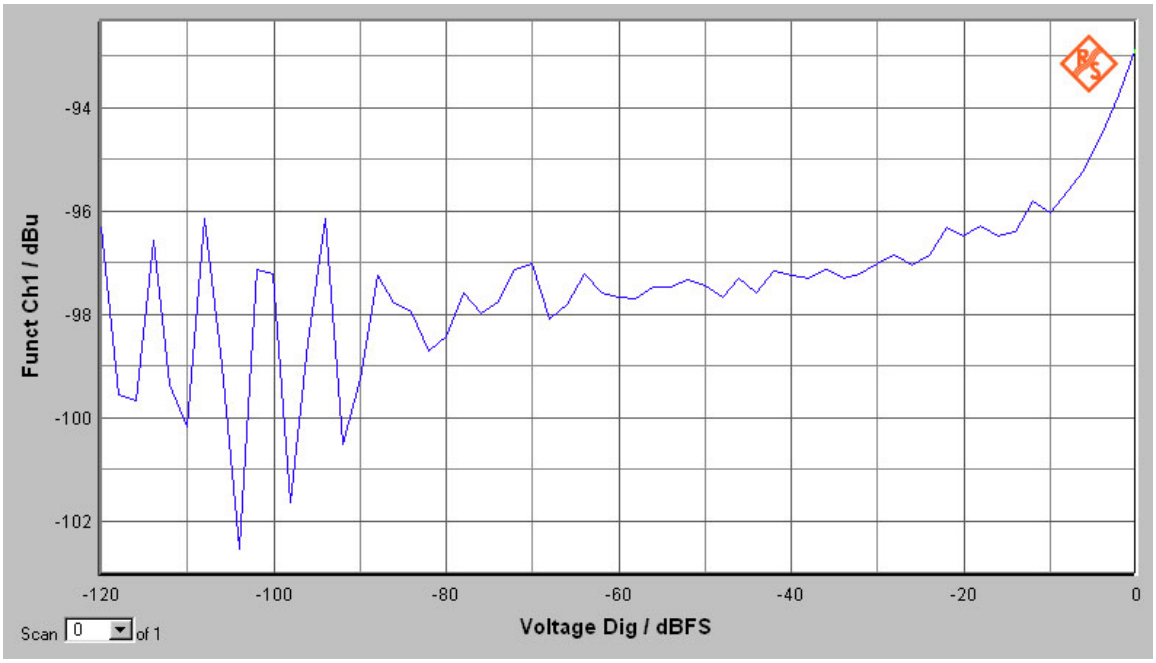


Figure 22. Noise level of the NTDA24 evaluation versus the power of the input signal when sample rate is 96kHz (A-Weighted, BW= 46kHz).

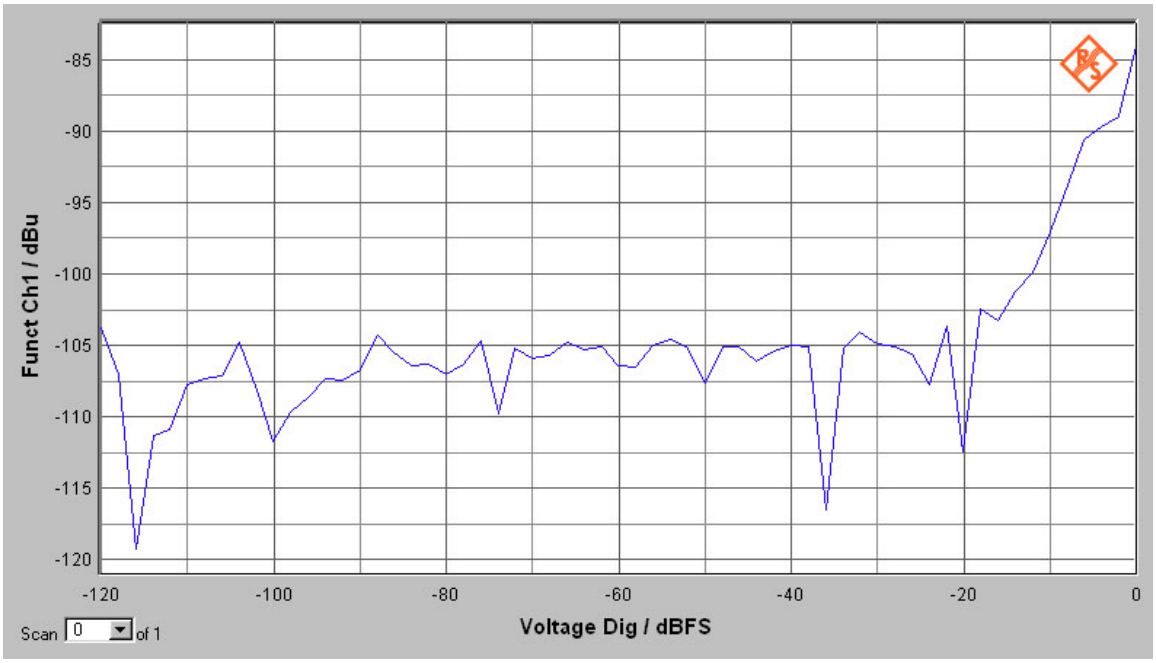


Figure 23. THD level of the NTDA24 evaluation versus the power of the input signal when sample rate is 96kHz (BW= 46kHz).

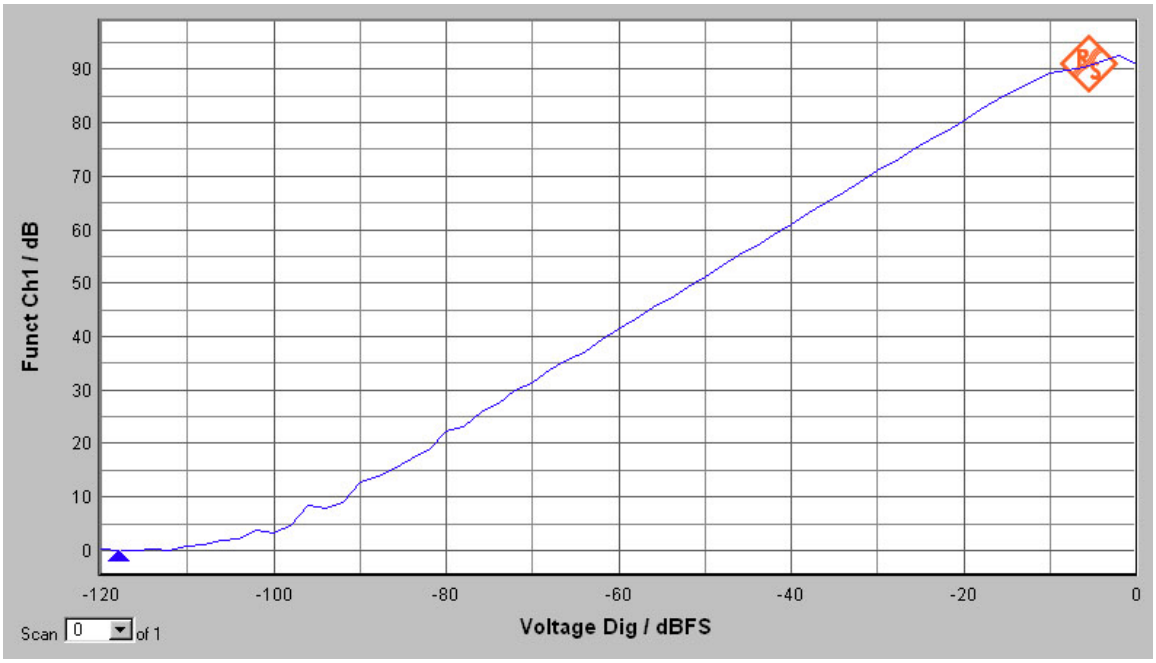


Figure 24. SNDR of the NTDA24 evaluation versus the power of the input signal when sample rate is 96kHz (BW= 46kHz). Note: The input FS signal level is 2Vrms so SFDR is 6dB higher than THD+Noise that is measured respect to 1Vrms reference level of UPV analyzer.

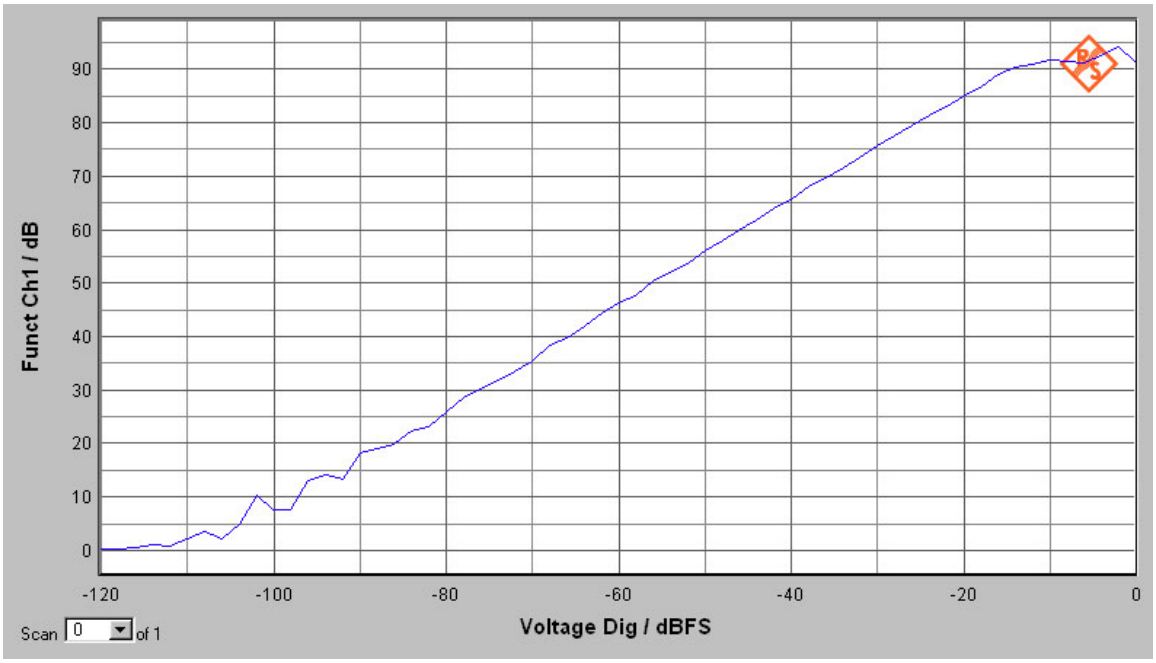


Figure 25. SNDR of the NTDA24 evaluation versus the power of the input signal when sample rate is 96kHz (A-Weighted, BW= 46kHz).

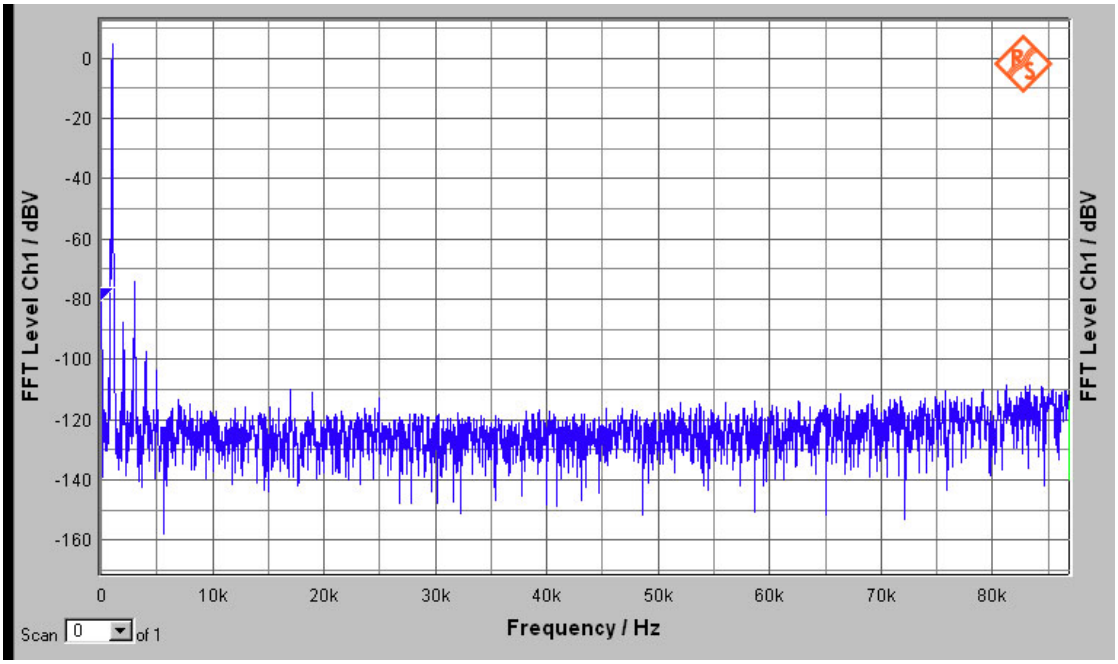


Figure 26. Output spectrum of the NTDA24 evaluation board for -1dBFS input signal and 192kHz sample rate.

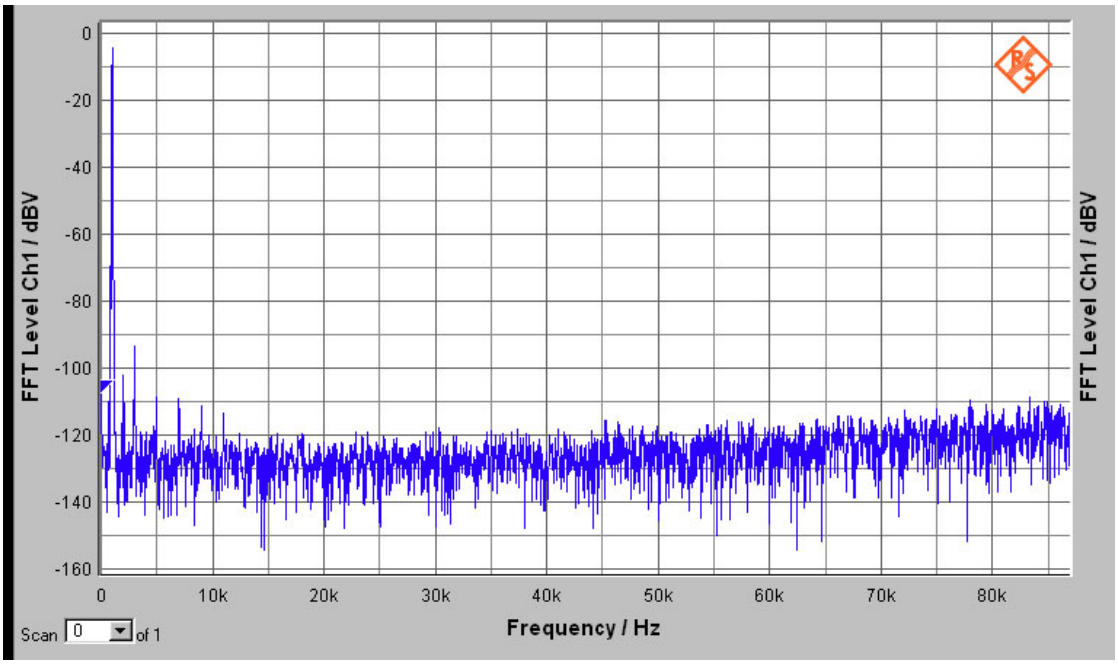


Figure 27. Output spectrum of the NTDA24 evaluation board for -10dBFS input signal and 192kHz sample rate.

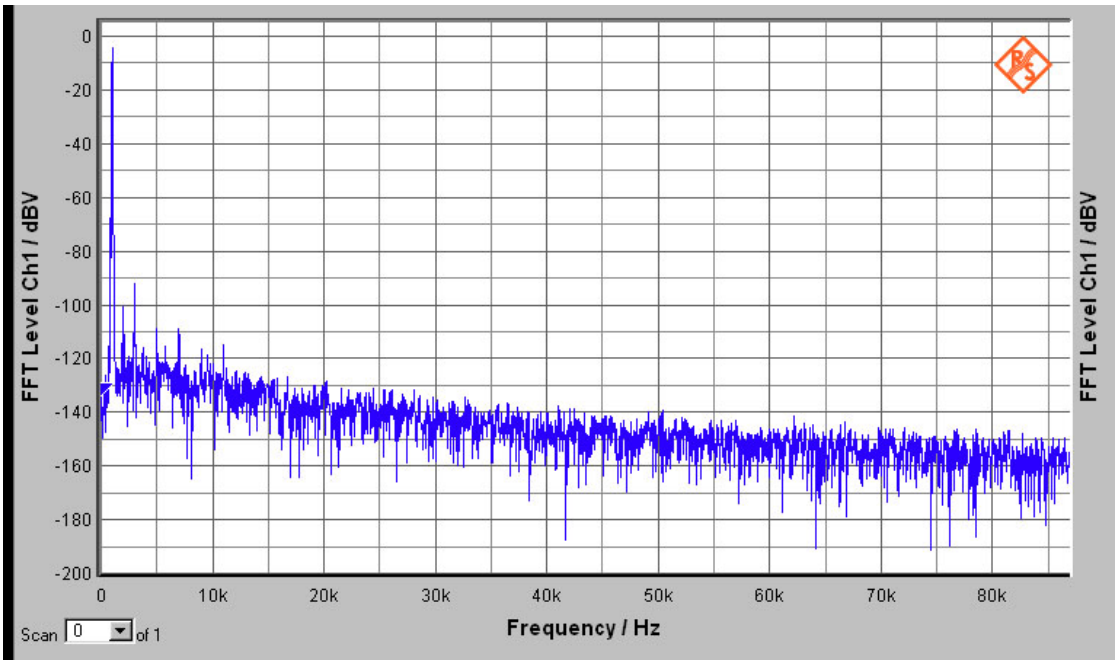


Figure 28. Output spectrum of the NTDA24 evaluation board for -10dBFS input signal and 192kHz sample rate (A-Weighted).

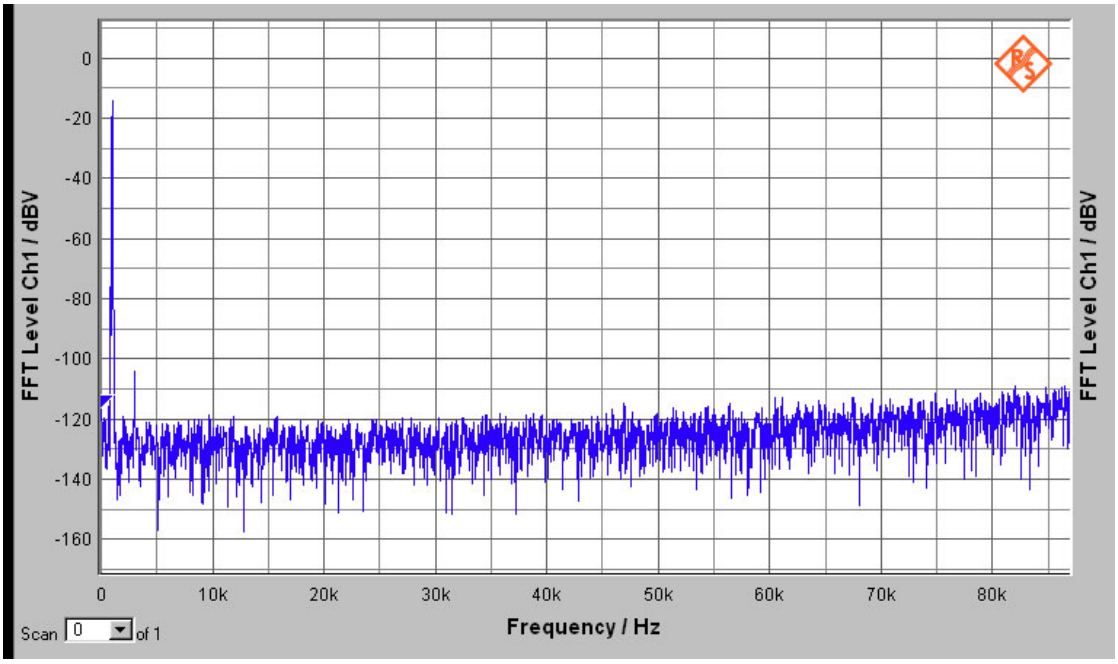


Figure 29. Output spectrum of the NTDA24 evaluation board for -20dBFS input signal and 192kHz sample rate.

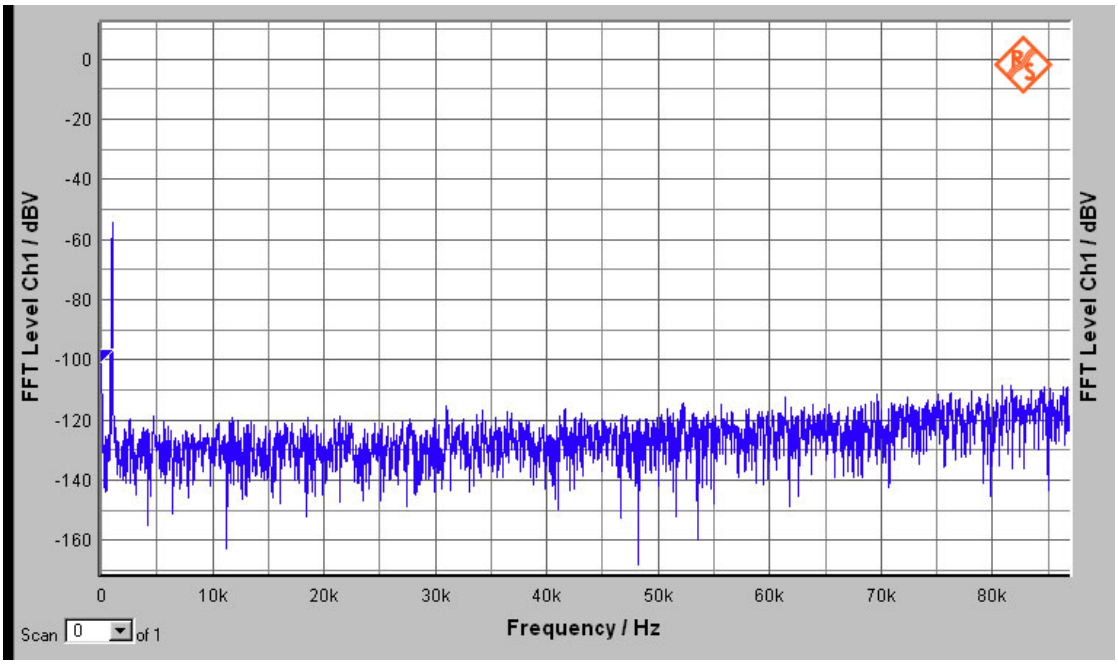


Figure 30. Output spectrum of the NTDA24 evaluation board for -60dBFS input signal and 192kHz sample rate.

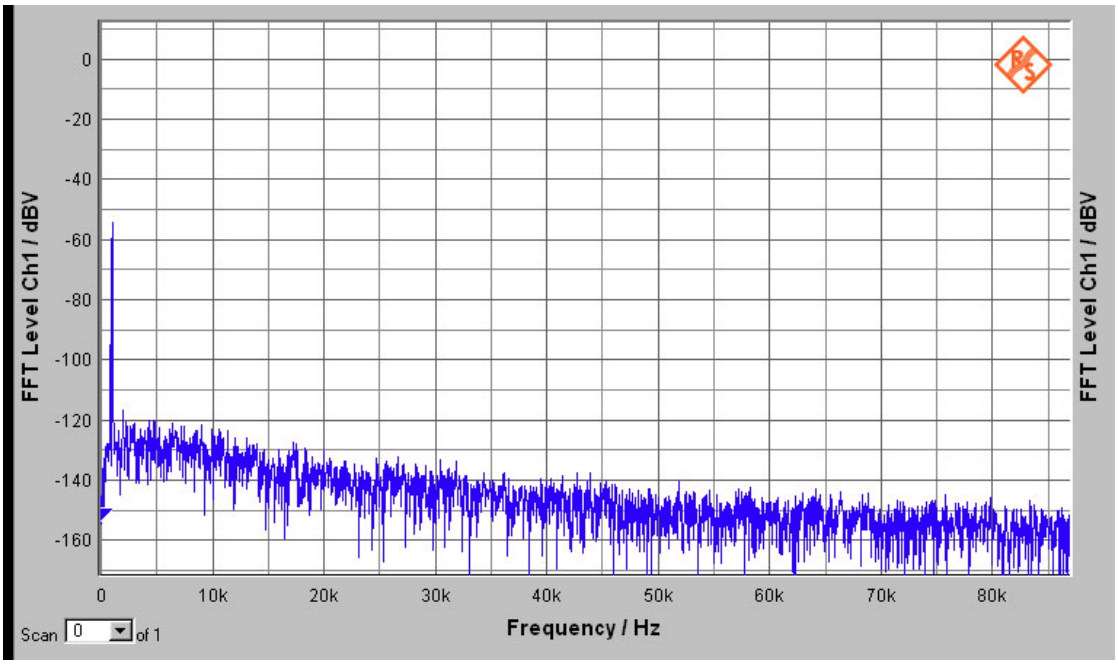


Figure 31. Output spectrum of the NTDA24 evaluation board for -60dBFS input signal and 192kHz sample rate (A-Weighted).

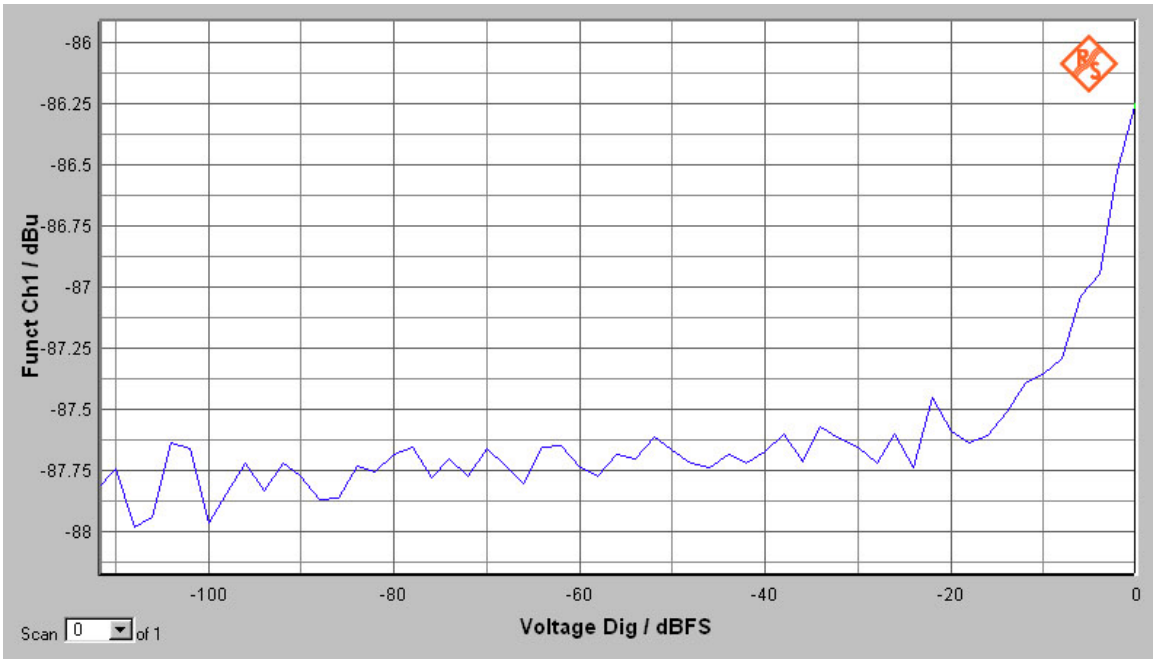


Figure 32. Noise level of the NTDA24 evaluation board versus the power of the input signal when sample rate is 192kHz (BW= 87kHz).

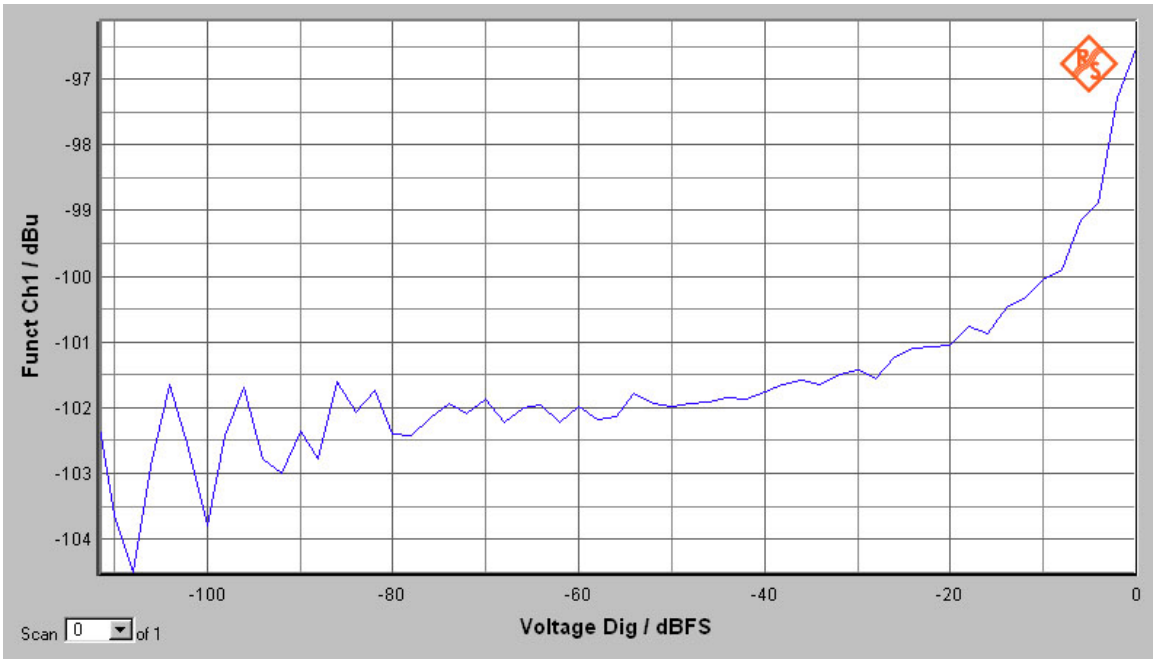


Figure 33. Noise level of the NTDA24 evaluation board versus the power of the input signal when sample rate is 192kHz (A-Weighted, BW= 87kHz).

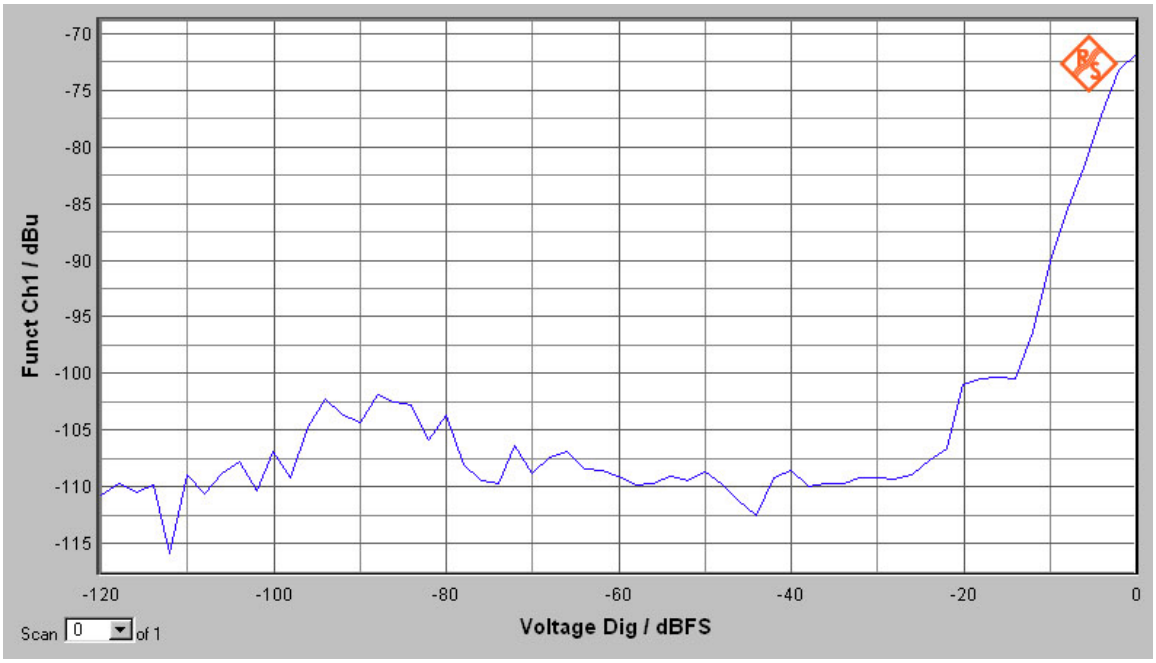


Figure 34. THD level of the NTDA24 evaluation board versus the power of the input signal when sample rate is 192kHz (BW= 87kHz).

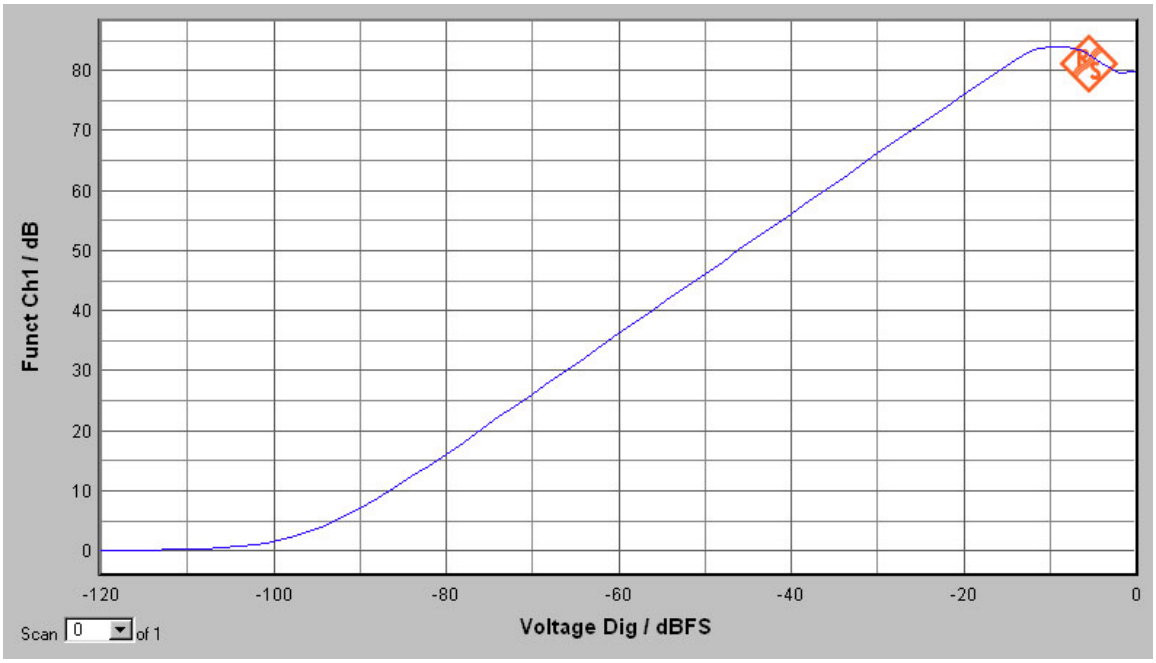


Figure 35. SNDR of the NTDA24 evaluation board versus the power of the input signal when sample rate is 192kHz (BW= 87kHz).

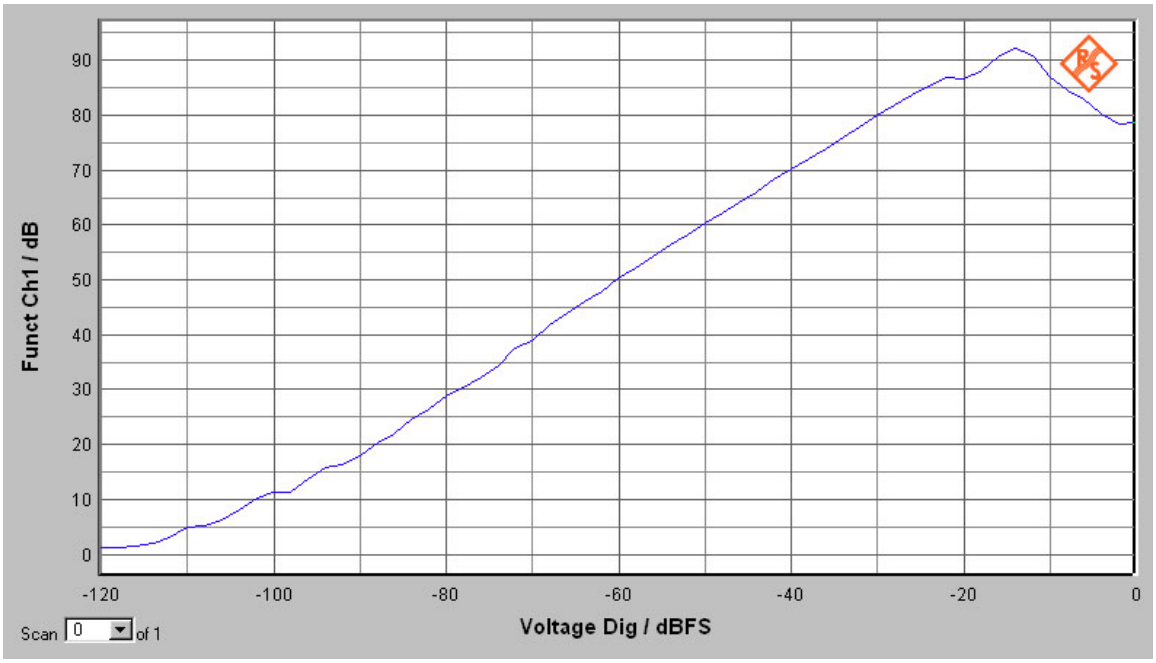


Figure 36. SNDR of the NTDA24 evaluation board versus the power of the input signal when sample rate is 192kHz (A-Weighted, (BW= 87kHz).

FUNCTIONAL DESCRIPTION

Device Architecture

The NTDA24 is a single channel mono DAC featuring multibit sigma-delta topology. The DAC is controlled by a bit-clock (BIT_CLK) and synchronization signal called LRClock.

General Overview

The NTDA24 is designed to run with an internal MCLK (MCLK) of 12.288 MHz and a modulator of 6.144 MHz. From this MCLK frequency, sample rates of 48 kHz, 96 kHz, and 192 kHz can be achieved on the channel. The internal clock should never be run at a higher frequency but may be reduced to achieve lower sampling rates. The modulator rate scales in proportion with the MCLK scaling.

OPERATING FEATURES

SPI Control Register Definitions

The NTDA24's Operating Mode is set by programming a Control Register via an SPI compatible port or via Pins. Table IV details the format of the NTDA24's Control Word, which is 16 bits wide with 3 reserved Bits (Bits 13 to 15).

Serial Data Interface

The NTDA24's serial data interface consists of three pins (LR_CLK, BIT_CLK, SERIAL_DATA_IN). LR_CLK is the framing signal for left and right channel samples and its frequency is equal to sampling frequency (f_s). BIT_CLK is the serial clock used to clock the data samples from the NTDA24 and its frequency is equal to $64 \times f_s$ (giving 32 BIT_CLK periods for each of the left and right channels). SERIAL_DATA_IN outputs the left and right channel sample data coincident with the falling edge of BIT_CLK.

The serial data output supports all the popular audio interface standards, such as I^2S, left-justified (LJ), and right-justified (RJ). The Interface Mode is selected by programming the Bits DF1-DF0 of Control Register (see Table II).

The data sample width can be selected from 16,20,24 bits by programming Bits WL1-WL0 of Control Register (see Table III).

I^2S Mode

In I^2S Mode, the data is left-justified, MSB first, with the MSB placed in the second BIT_CLK period following the transition of the LR_CLK. A high-to-low transition of the LR_CLK signifies the beginning of the left channel data transfer, while a low-to-high transition on the LR_CLK signifies the beginning of the right channel data transfer (see Figure 10)

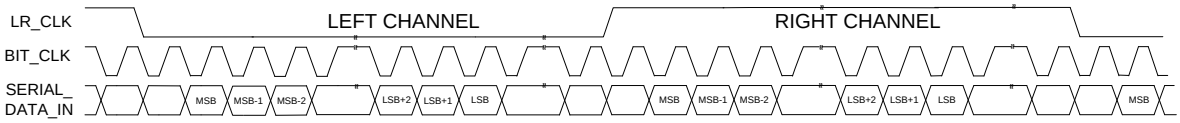


Figure TCP 7. I^2S Mode

Left-Justified Timing

In LJ Mode, the data is left-justified, MSB first, with the MSB placed in the first SCLK period following the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the right channel data transfer, while a low-to-high transition on the LRCLK signifies the beginning of the left channel data transfer (see Figure 11)

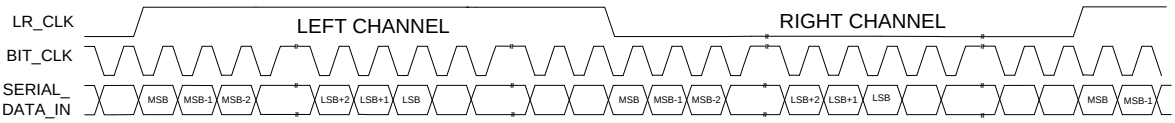


Figure TCP 8. LJ Mode

Right-Justified Timing

In RJ Mode, the data is right-justified, LSB last, with the LSB placed in the last SCLK period preceding the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the right channel data transfer, while a low-to-high transition on the LRCLK signifies the beginning of the left channel data transfer (see Figure 12)

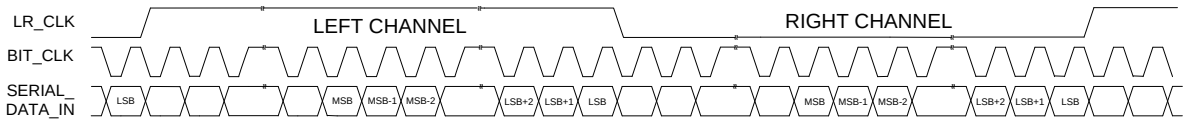


Figure TCP 9. RJ Mode

TEST METHOD & CONFIGURATIONS

General Description

The test is performed using the configuration setup shown in the following figure. The NTDA24 evaluation board provides a means for evaluating the NTDA24, 24-bit mono DAC. Evaluation requires a digital signal source, an analog signal analyzer, and a power supply. Also included is a CS8416 digital audio receiver which receives S/PDIF, and EIAj-340 compatible audio data and makes standard serial data readable by NTDA24. The input digital data of CS8416 is supplied via BNC and or optical connectors. The FPGA Board (Stratix II EP2S60 DSP Development Board) programs the NTDA24 EVB with a NikTek Semiconductor programming code. The digital output data from CS8416 EVB is captured by means of the FPGA Board. The analog output of NTDA24 EVB is digitized by NTAD24 EVB (NTAD24 Evaluation board) or a third party 24-bit ADC evaluation board. The captured data is transferred to a PC and evaluated using NikTek Semiconductor analysis codes. It should be mentioned that programming of the FPGA Board and data logging is performed by Altera's Quartus® II software.

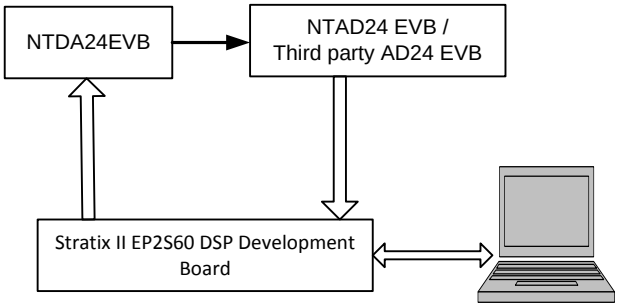


Figure S1. Test Configuration

List of Equipments

Type	Notes
NTDA24 Evaluation Board	The Main Board
Stratix II EP2S60 DSP Development Board	1) Programming the NTDA24 EVB 2) Capturing the CS8416 Digital Audio Receiver's digital output data
CS8416 Digital Audio Receiver	Receives S/PDIF, and EIAj-340 compatible audio data and makes standard serial data readable by NTDA24
+5V & ±15V Rechargeable Batteries	Used as clean power supplies for NTDA24 EVB and NTAD12100 EVB
100Msps Oscilloscope + Multimeter a) 4-wire SMA Cable b) 4-wire SMA Cable c) XLR Cable	Checking the intermediate signals a) Connecting 4-pin headers from FPGA board to NTDA24 Evaluation board b) Connecting NTAD24 EVB to FPGA board c) Connecting NTDA24 EVB to CS8416 Digital Audio Receiver

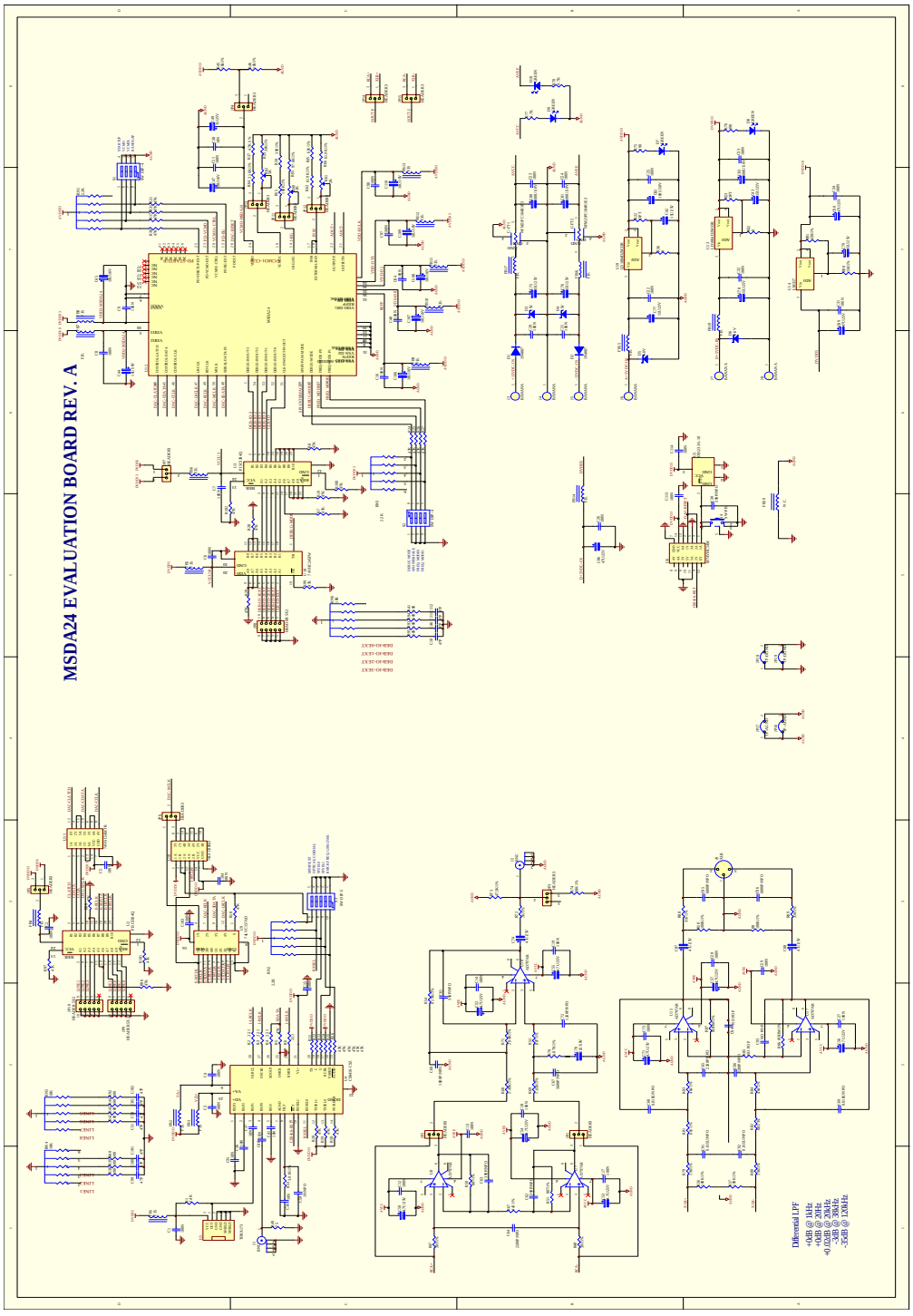


Figure S2. The Schematic of the evaluation board

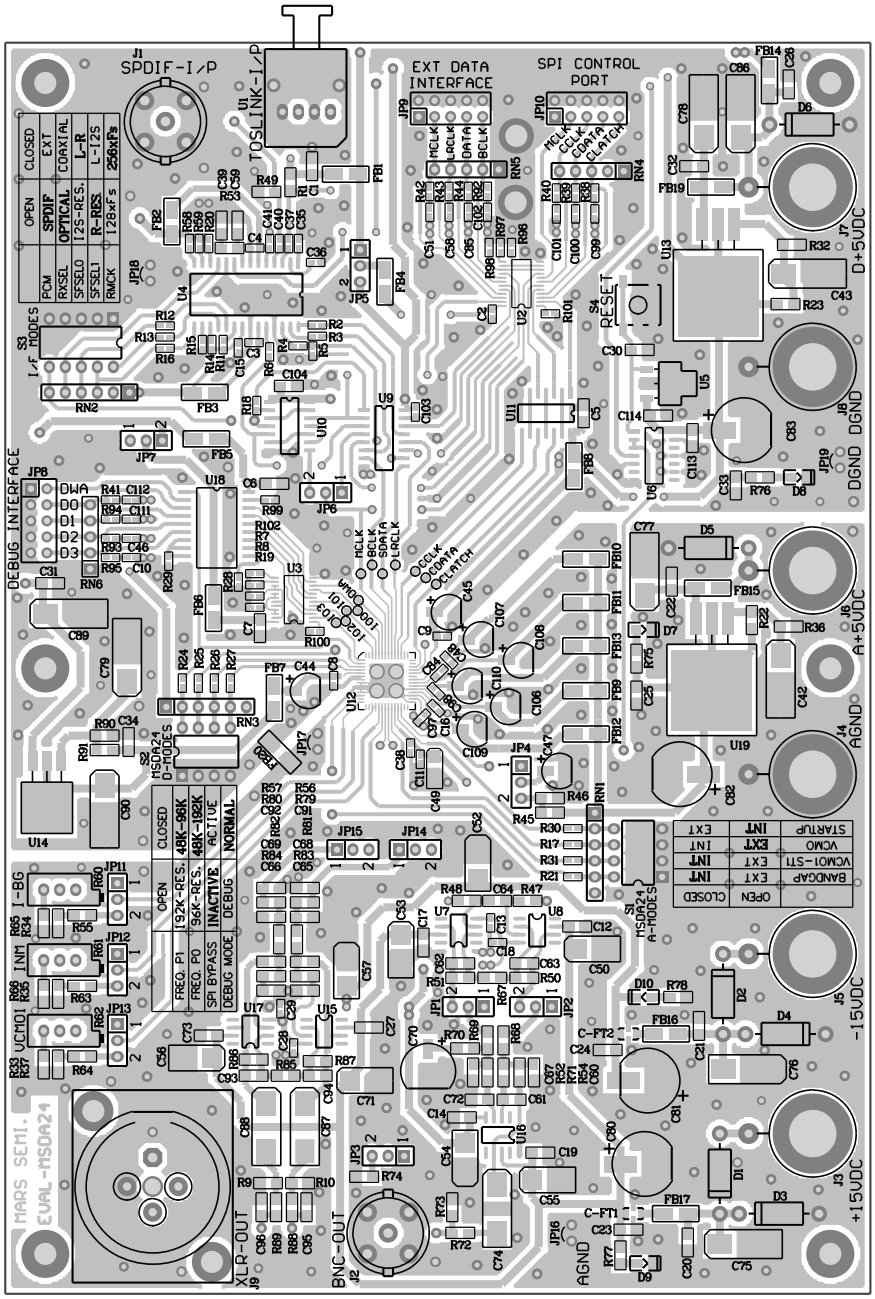


Fig. S3. Top layer of the PCB board.

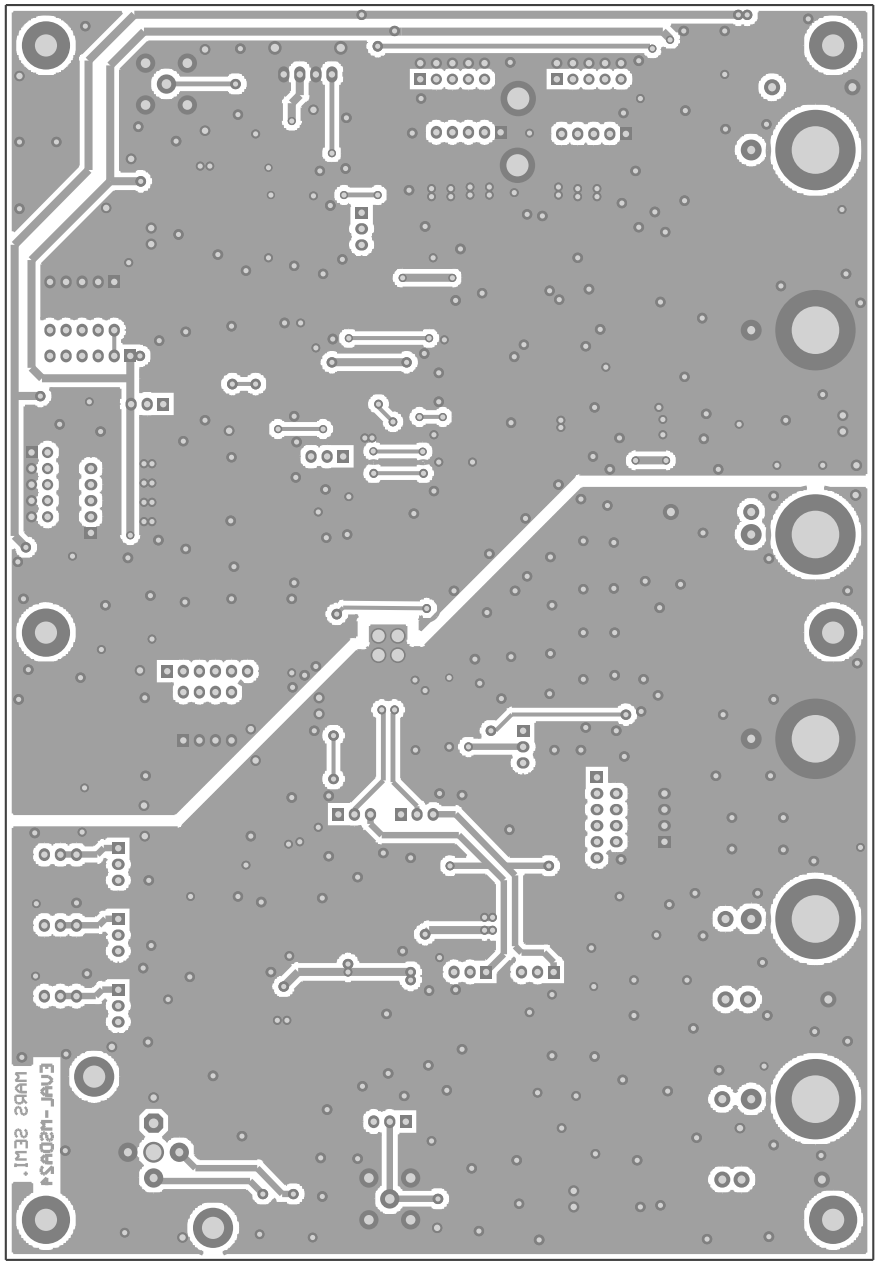
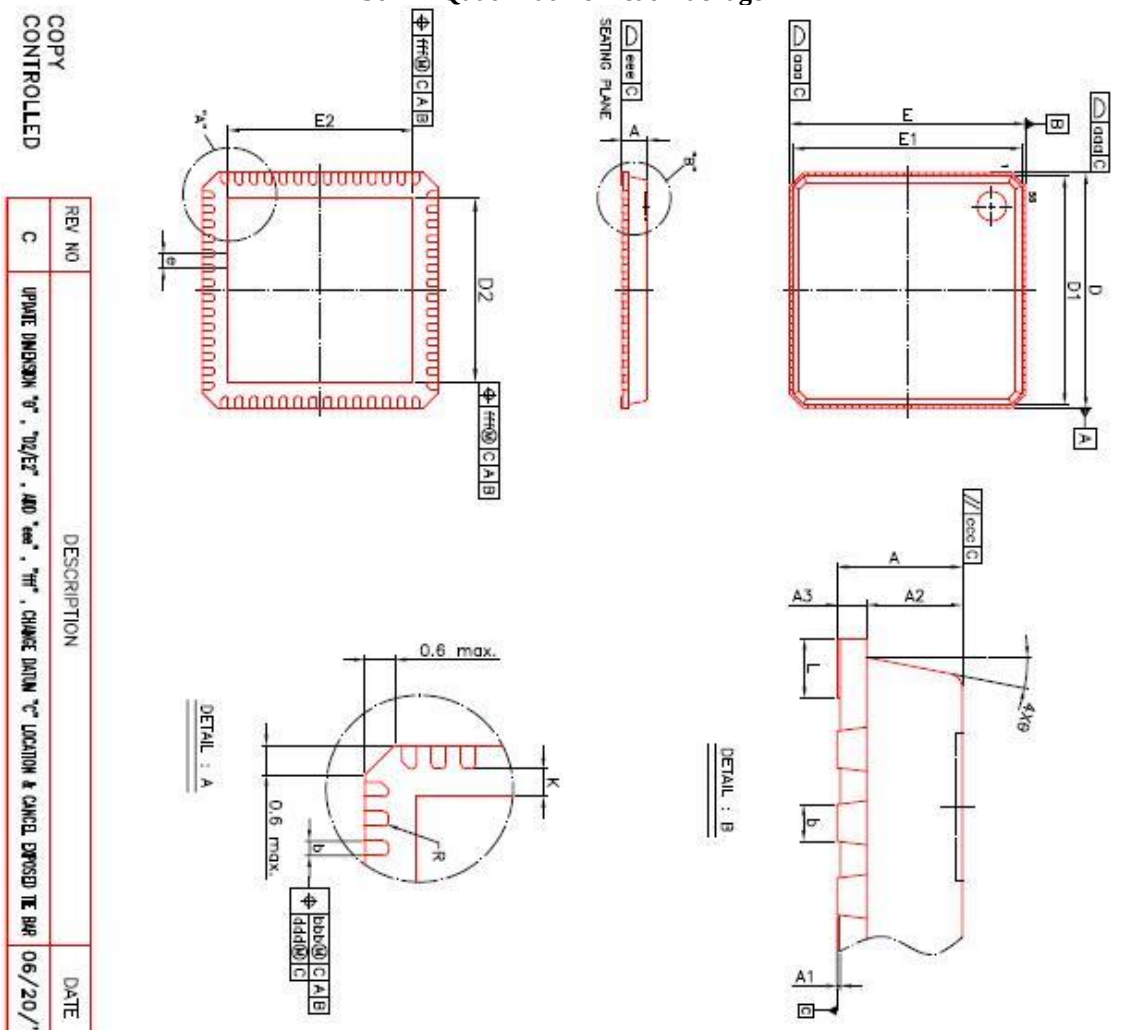


Fig. S4. Bottom layer of the PCB board.

OUTLINE DIMENSION

56 Pin Quad Flat No-Lead Package



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		8.00 BSC			0.315 BSC	
D1/E1		7.75 BSC			0.305 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	----	14°	0°	----	14°
R	0.09	----	----	0.004	----	----
K	0.20	----	----	0.008	----	----
aaa	----	----	0.15	----	----	0.006
bbb	----	----	0.10	----	----	0.004
ccc	----	----	0.10	----	----	0.004
ddd	----	----	0.05	----	----	0.002
eee	----	----	0.08	----	----	0.003
fff	----	----	0.10	----	----	0.004

L/F	Exposed Pad Size D2/E2 (mm)			D2/E2 (inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
①	4.22	4.37	4.52	0.166	0.172	0.178
②	5.90	6.05	6.20	0.232	0.238	0.244

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

COPY CONTROLLED

REV NO	DESCRIPTION	DATE
C	UPDATE DIMENSION "G", "D2/E2", AND "eee", "fff", CHANGE DATUM "C" LOCATION & CANCEL EXPOSED TIE BAR	06/20/'05

TITLE : 56LD QFN (8X8 mm) PACKAGE OUTLINE			
L/F MATERIAL : A194 FH			
APPR.	F.D.Tong	DWG NO.	CE056-SW1
ENG.	Albert Lee Terry Tsai	REV NO.	C
QM.	S.T.Liao	PRODUCT CODE	CE0563A , CE0561B KB0561A , KB0562B
CHK.	Y.Y.Lai	DATE	06/20/'05
DWG.	R.K.Wang	SHT No.	1/1
SILICONWARE PRECISION INDUSTRIES CO., LTD.			