Mono, 24-Bit, 48/96/192 kHz Multibit ΣΔ ADC

FEATURES

3.3 V Mono Audio ADC System
    with 1.8 V Digital Interfaces and Circuitry
Multi-Bit Sigma-Delta Modulator
Support 16-/20-/24-Bit Word Lengths
Support 48/96/192 kHz Sample Rates
On-Chip Reference Voltage Buffer
Differential Input for Optimum Performance
3.3 V_{p-p} Differential Analog Input Voltage
-96dB THD+Noise (A-weighted)
112 dB Dynamic Range (A-weighted)
35 mW Typical Power Consumption at 48 kHz
Flexible Serial Data Port
    Allows Right-Justified, Left-Justified, and I^2S
Die Area [mm^2]
    Analog Core: 2.8×3
    Digital Core: 2.2×3
Device Control via SPI Compatible Serial Port or
    Optional Control Pins

APPLICATIONS

High-end Audio/Video Amplifiers and Receivers
Professional Audio
Mixing Consoles
Musical Instruments
Digital Audio Recorders, Including CD-R, MD, DVD-R, DAT, HDD
Home Theater Systems
Automotive Audio Systems
Multimedia
Digital Audio Effects Processors

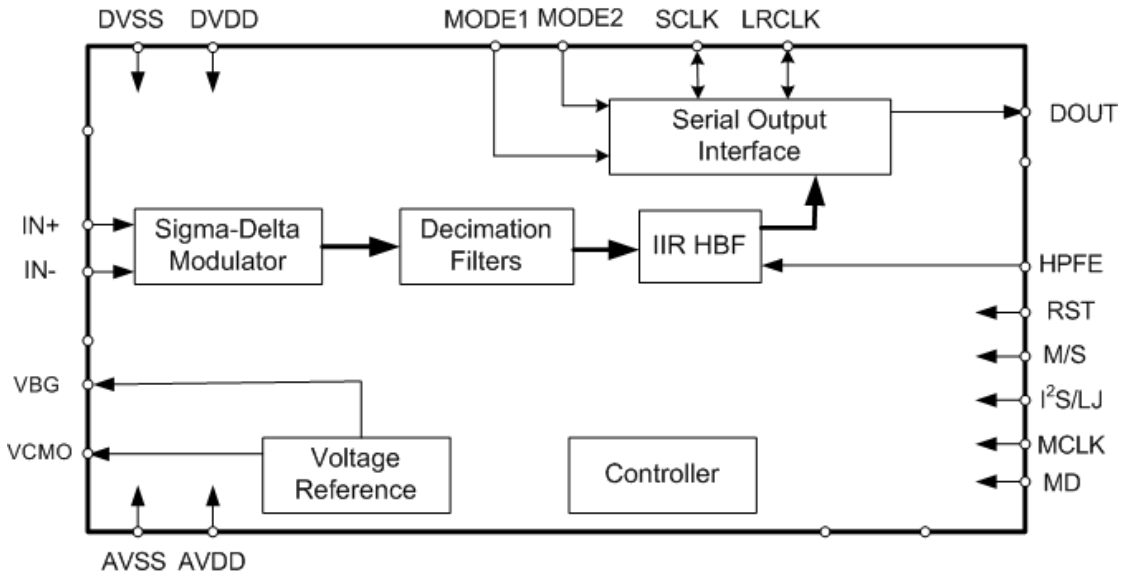
PRODUCT DESCRIPTION

The NTAD24 is a monolithic 24-bit Audio analog-to-digital converter and is optimized for digital audio systems. It provides a wide dynamic range, generating 16-/20-/24-bit values for both left and right inputs in serial form at sample rates up to 192kHz per channel*. It offers a wide dynamic range, negligible distortion and low thermal and flicker noise.

The NTAD24 uses a third-order multi-bit delta-sigma modulator, followed by selectable decimation filters to support 48/96/192 kHz output sample rates, high-pass filtering, and offset cancellation. Each channel provides 102.4 dB of dynamic range and 88.7 dB SNDR suitable for applications such as digital audio recorders and mixing consoles. The decimation filter response features very low passband ripple (less than 0.0025 dB) and excellent stop-band attenuation (more than 120 dB). The NTAD24 operates with 3.3 V analog power supply and 1.8 V digital power supply with ±5% power supply tolerances. It is housed in a 56-lead QFN Plastic Package and is characterized for operation over the temperature range –40°C to +85°C.

* Although the DSP is designed for stereo audio, the analog is single channel in this prototype chip.

FUNCTIONAL BLOCK DIAGRAM



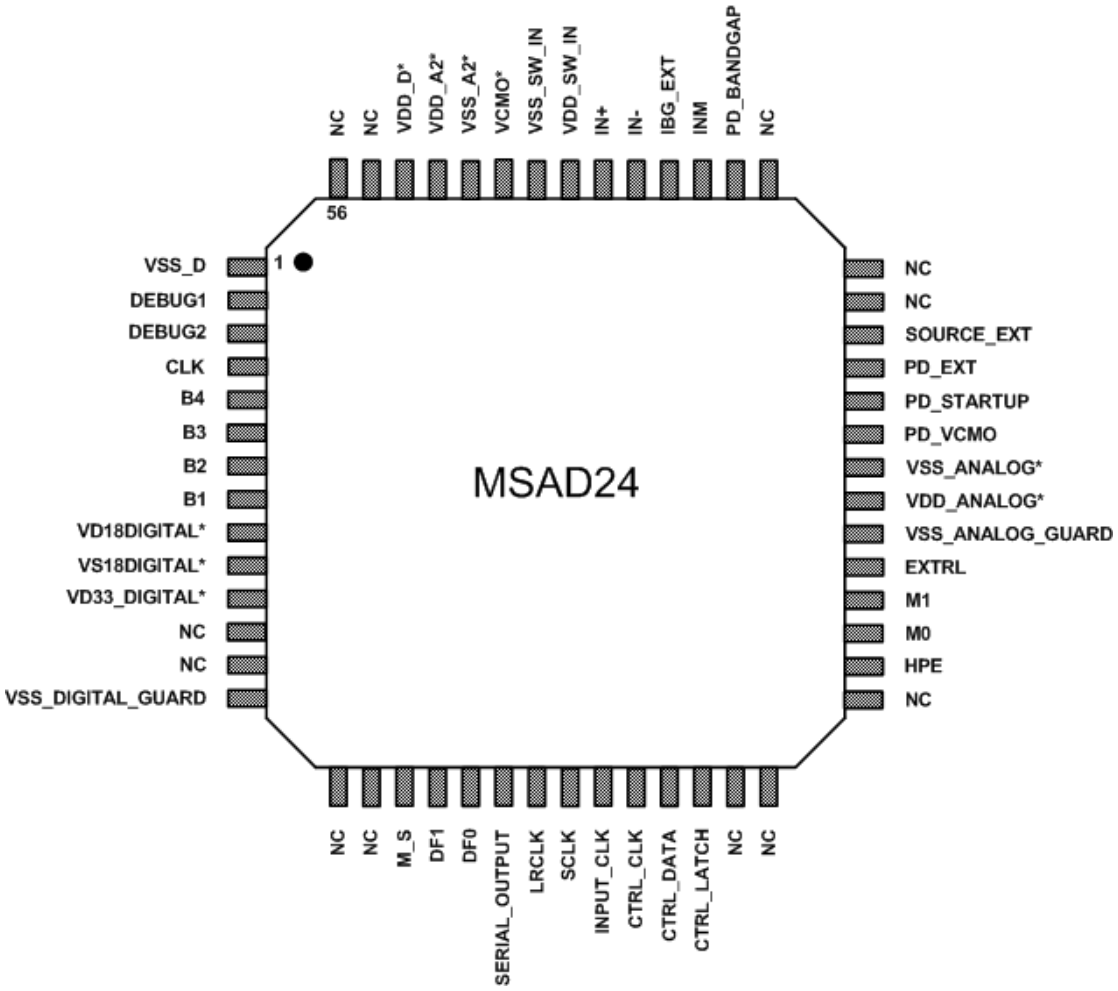
NTAD24-SPECIFICATIONS

TEST CONDITION UNLESS OTHERWISE NOTED

Supply Voltage (AV_{DD}/DV_{DD})	3.3/1.8 V
Ambient Temperature	25°C
Input Clock	12.288 MHz
Input Signal	997 Hz
Measurement Bandwidth	20 Hz to 22.5 kHz
Word Length	24 Bits
Master Mode, Data I^2S Justified	

Parameter	Min	Type	Max	Unit	Test Condition
ANALOG PERFORMANCE					
Dynamic Range (A-weighted)		112		dB	**20 Hz to 22.5 kHz -60 dBFS**
Total Harmonic Distortion+Noise (A-weighted)		-96		dB	**20 Hz to 22.5 kHz -4 dBFS**
ANALOG INPUT					
Differential Input Range, p-p (Full Scale)		6.6		Vpp,diff	
Input Mode Voltage		1.65		V	
Input Impedance		1.3		kΩ	
ADC DECIMATION FILTER (48 kHz)					
Decimation Factor		128		-	
Pass Band		21.77		kHz	
Pass-Band ripple		±0.0025		dB	
Stop Band	26.23			kHz	
Stop-Band Attenuation	120			dB	
Group Delay		820		µs	
ADC DECIMATION FILTER (92 kHz)					
Decimation Factor		64		-	
Pass Band		43.54		kHz	
Pass-Band ripple		±0.0025		dB	
Stop Band	52.48			kHz	
Stop-Band Attenuation	120			dB	
Group Delay		410		µs	
ADC DECIMATION FILTER (192 kHz)					
Decimation Factor		32		-	
Pass Band		65.31		kHz	
Pass-Band ripple		±0.0025		dB	
Stop Band	78.69			kHz	
Stop-Band Attenuation	120			dB	
Group Delay		206		µs	
HIGH-PASS DIGITAL FILTER (f_S=48 kHz)					
Cutoff Frequency		1		Hz	
HIGH-PASS DIGITAL FILTER (f_S=96 kHz)					
Cutoff Frequency		2		Hz	
HIGH-PASS DIGITAL FILTER (f_S=192 kHz)					
Cutoff Frequency		4		Hz	
POWER SUPPLY					
Supply Voltage (Analog)		**3.3**		**V**	
Supply Voltage (Digital1)		**1.8**		**V**	
Supply Voltage (Digital2)		**3.3**		**V**	**Used for ESD Protection**
Supply Current (Analog)		**10**		**mA**	
Supply Current (Digital)		**1.1**		**mA**	

PIN CONFIGURATION



Pin No.	Mnemonic	Input/ Output	Description
1	VSS_D	Power	Ground supply (0V), mixed analog-digital
2	DEBUG1	I	Debug mode1 (normal=0 , debug mode=1)
3	DEBUG2	I	Debug mode2 (normal=0, debug mode=1)
4	CLK	I/O	Capture clock (output if DEBUG1=0, input if DEBUG1=1)
5	B4	I/O	Digital output (DEBUG2=0), Digital input (DEBUG2=1)
6	B3	I/O	
7	B2	I/O	
8	B1	I/O	
9	VD18DIGITAL*	Power	Positive digital supply (1.8 V)
10	VS18DIGITAL*	Power	Digital ground
11	VD33_DIGITAL*	Power	Positive digital supply (3.3 V)
12	NC	—	———
13	NC	—	———
14	VSS_DIGITAL_GUARD	Power	Digital guard ring ground
15	NC	—	———
16	NC	—	———
17	M_S	I	Master/Slave select is used to select between master (pin

			low) or slave (pin high) modes
18	DF1	I	Audio serial data output format (refer to Table2)
19	DF0	I	
20	SERIAL_OUTPUT	O	Audio serial output, MSB first, containing two channels of 16/20/24 bit two's complement data
21	LRCLK	IO	Left/Right clock determines which channel is active on the serial data output [Output when 'M/S'=0 (default); Input when 'M/S=1]
22	SCLK	I/O	Audio serial bit clock which determines the rate of audio data transfer (1.5 MHz); [Output when 'M/S'=0 (default); Input when 'M/S=1]
23	INPUT_CLK	I	Master Clock for Delta-Sigma modulator and digital filters (12.288 MHz)
24	CTRL_CLK	I	Clock signal for control port (SPI) interface
25	CTRL_DATA	I	Control port data input- serial data input for control port (SPI) interface. MSB first, containing 16 bit of unsigned
26	CTRL_LATCH	I	Frame sync (framing signal) for control port (SPI) interface
27	NC	—	———
28	NC	—	———
29	NC	—	———
30	HPE	I	High Pass filter Enable [0=Disable (Default), 1=Enable]
31	M0	I	Frequency mode selection (output sample rate) (refer to Table1)
32	M1	I	
33	EXTRL	I	SPI interface enable (0 enables SPI interface; 1 chooses the control pins instead: 24-26, 34-36)
34	VSS_ANALOG_GUARD	Power	Analog ground (0 V), no. 1
35	VDD_ANALOG*	Power	Positive analog supply (3.3V), no. 1
36	VSS_ANALOG*	Power	Analog ground (0 V), no. 2
37	PD_VCMO	I	VCMO power down (Normal=0 V, External VCMO=3.3 V)
38	PD_STARTUP	I	STARTUP power down (Normal=0 V, External STARTUP= 3.3 V)
39	PD_EXT	I	Power down, common between analog and digital parts and also is used for digital system reset (Normal=0 V, power down mode= 3.3 V)
40	SOURCE_EXT	A/IO	Pin connected to external R=1 K□ to generate Bandgap current
41	NC	—	———
42	NC	—	———
43	NC	—	———
44	PD_BANDGAP	I	Bandgap power down (Normal=0 V, External Bandgap Overwrite= 3.3 V)
45	INM	A/IO	Pin connected to both external Resistors R=1 K□ & R=62.5 K□ to generate Bandgap current
48	IBG_EXT	A/IO	Back-up external bandgap current
47	IN-	A/I	Negative input
48	IN+	A/I	Positive input
49	VDD_SW_IN	Power	Positive analog supply (3.3V), no. 2
50	VSS_SW_IN	Power	Analog ground (0 V), no. 3
51	VCMO*	A/IO	VCMO voltage connected to external capacitor=47uF (externally VCMO can also be forced)
52	VSS_A2*	Power	Negative analog reference voltage (0 V)
53	VDD_A2*	Power	Positive analog reference voltage (3.3 V)

54	VDD_D*	Power	Positive supply (3.3V), mixed analog-digital
55	NC	—	———
56	NC	—	———

Table 1. Mode Selection

M1	M0	Mode Selection
0	0	**Single speed (f_{sout}=48 KHz)**
0	1	**Double speed (f_{sout}=96 KHz)**
1	0	**Quad speed (f_{sout}=192 KHz)**
1	**1**	**reserved**

Table 2. Data Format

DF1	DF0	Data Format
0	0	**I^2s (default)**
0	1	**Left-Justified**
1	0	**Right-Justified**
1	**1**	**reserved**

Table 3. SPI (CIN) Control Register

15-10	9	8	7	6	5	4	3	2	1	0
Reserved	WW1	WW0	MUR	MUL	M/S	DF1	DF0	M1	M0	HPE

9	WW1	Word Width (See Table 4)
8	WW0	
7	MUR	Mute Control Right Channel (0 = Disabled (Default); 1 = Enabled)
6	MUL	Mute Control Left Channel (0 = Disabled (Default); 1 = Enabled)
5	M/S	Master/Slave Select (0 = Master Mode (Default); 1 = Enabled)
4	DF1	Data Format (See Table 2)
3	DF0	
2	M1	Mode Selection (See Table 1)
1	M0	
0	HPE	High-Pass Filter Enable (0 = Disabled (Default); 1 = Enabled)

Table 4. Word Width

WW1	WW0	Word Width (No. of Bits)
0	0	**24 (Default)**
0	1	**20**
1	0	**16**
1	**1**	**Reserved**

TERMINOLOGY

Dynamic Range

The ratio of a full-scale input signal to the integrated input noise in the desired bandwidth (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a -60 dB input signal and is equal to (S/[THD+N])+60 dB. Note that spurious harmonics are below the noise with a -60 dB input, so the noise level describes the dynamic range.

Total Harmonic Distortion + Noise

Rms sum of the all spectral components in pass band, excluding the signal power. Expressed in decibles. Measured respect to -8dBFS here.

Pass band

The region of the frequency spectrum unaffected by the attenuation of the digital decimation filter

Pass band Ripple

The peak to peak variation in amplitude response from equal-amplitude input signal frequencies within the pass band, expressed in decibels..

Stop Band

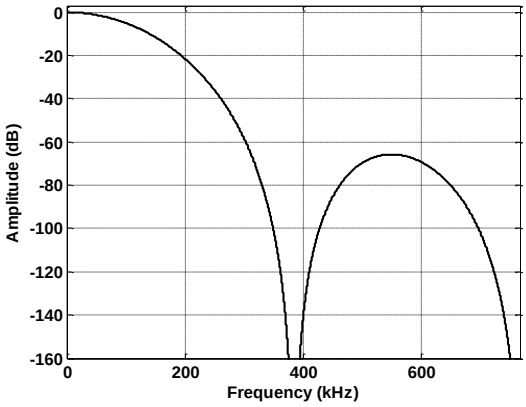
The region of the frequency spectrum attenuated by the digital decimation filter to the degree specified by the stop-band attenuation.

Group Delay

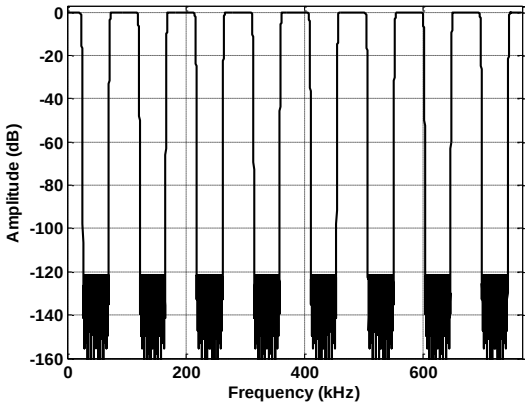
The time interval required for an input pulse to appear at the converter's output, expressed in millisecond (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

NTAD24-Typical Performance Characteristics

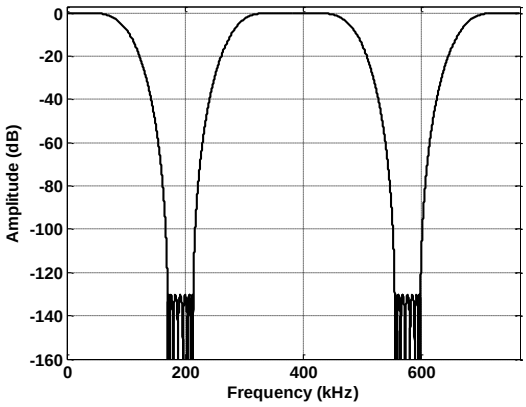
FILTER RESPONSES



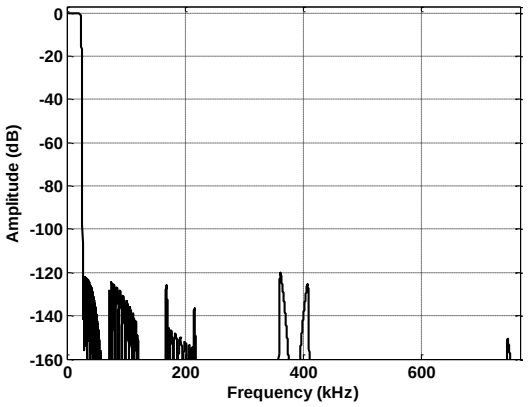
TCP 1. Sinc Filter Response



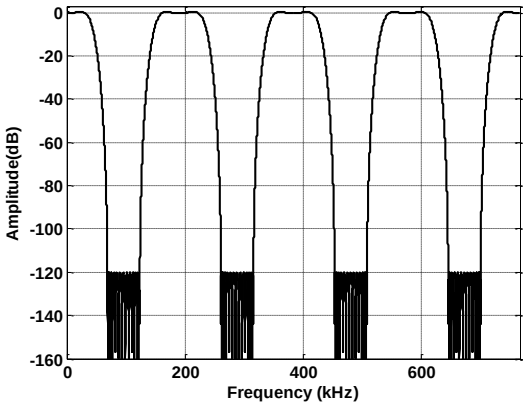
TCP 4. Second Half-Band Filter Response



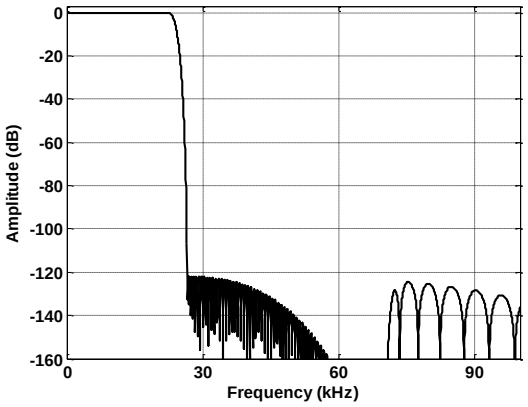
TCP 2. First Half-Band Filter Response



TCP 5. Composite Filter Response



TCP 3. Droop Correction Filter Response



TCP 6. Composite Filter Response (Pass Band Section)

NTAD24 MEASUREMENTS RESULTS

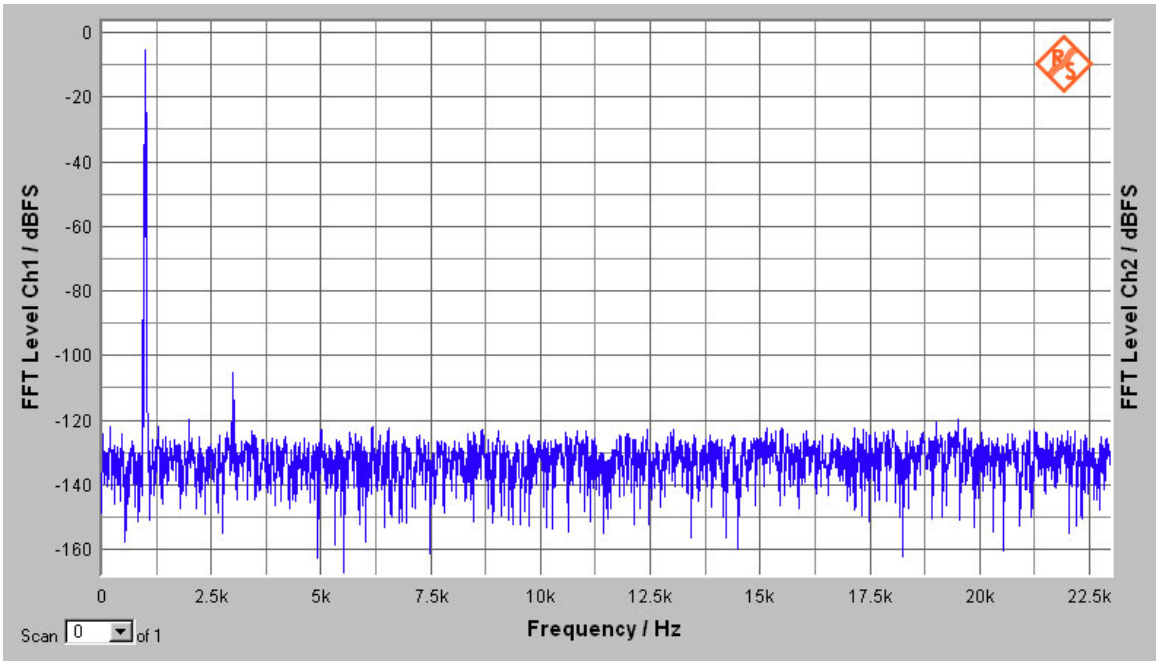


Figure 1. Output spectrum of the NTAD24 evaluation board for -4dBFS input signal and 48kHz sample rate.

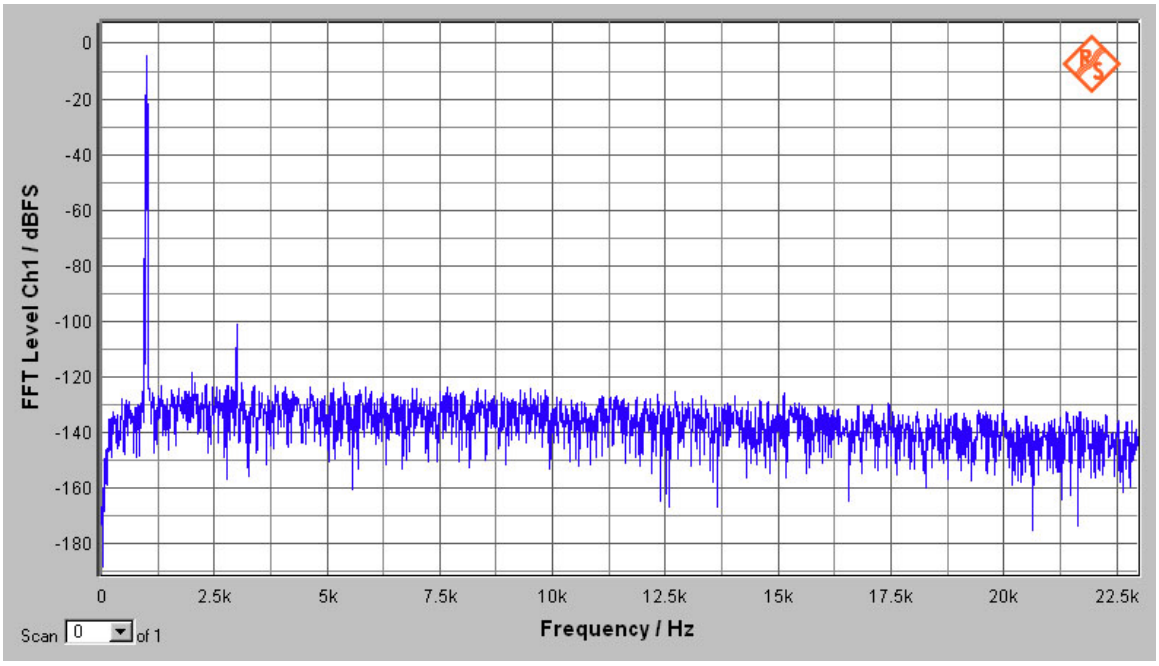


Figure 2. Output spectrum of the NTAD24 evaluation board for -4dBFS input signal and 48kHz sample rate (A-Weighted).

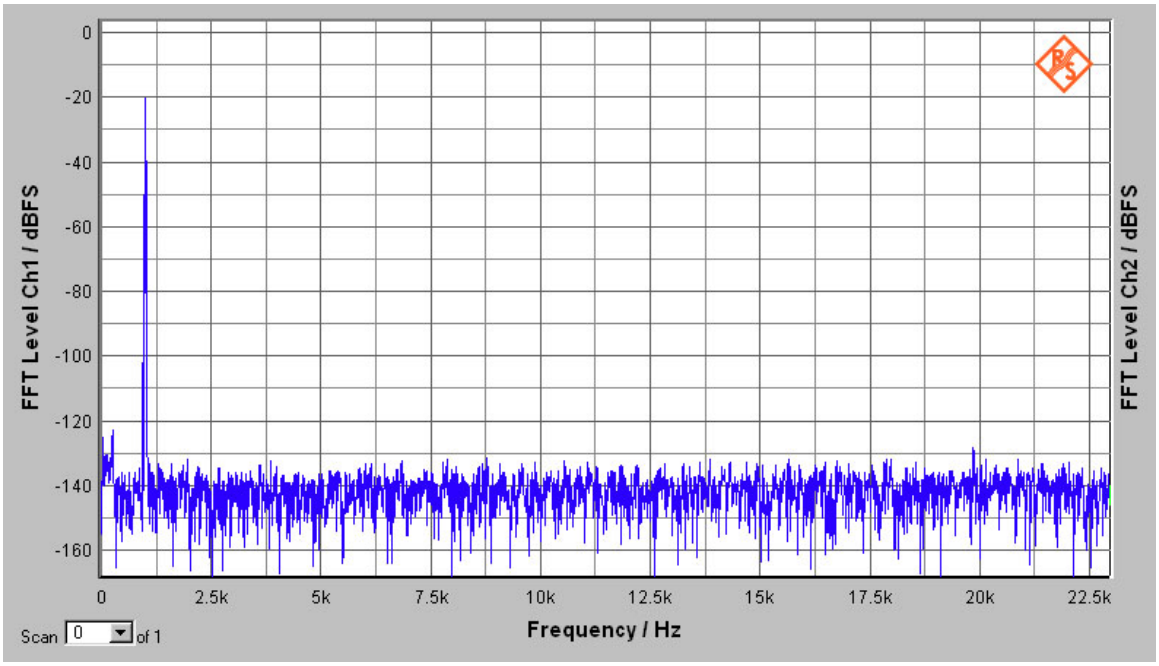


Figure 3. Output spectrum of the NTAD24 evaluation board for -20dBFS input signal and 48kHz sample rate.

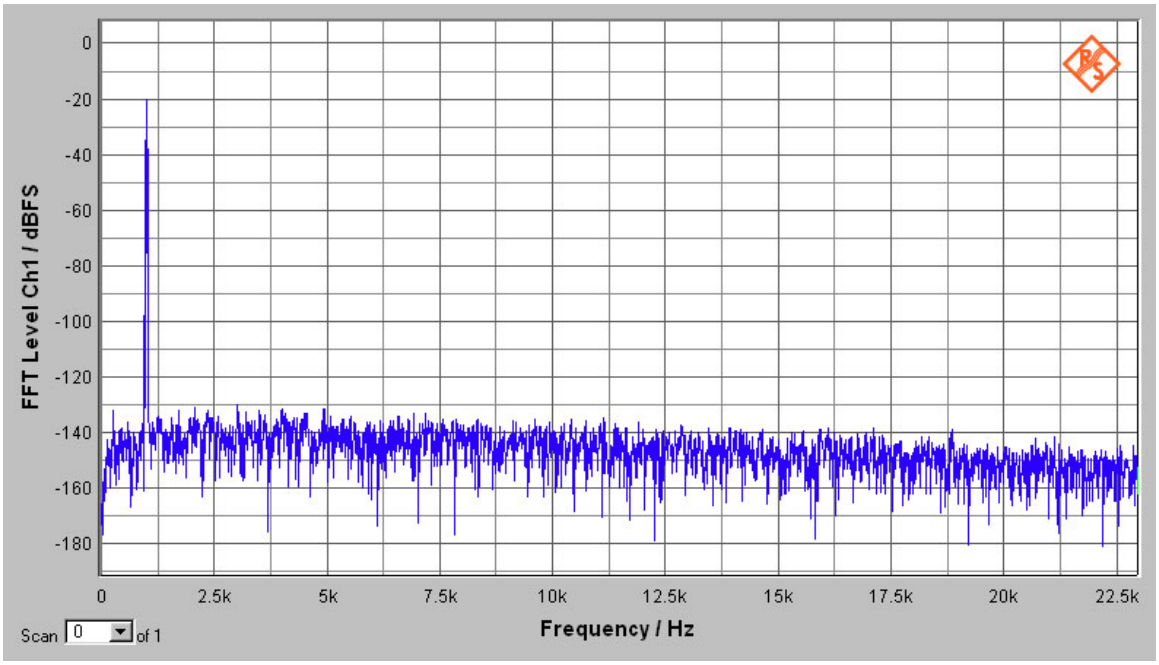


Figure 4. Output spectrum of the NTAD24 evaluation board for -20dBFS input signal and 48kHz sample rate (A-Weighted).

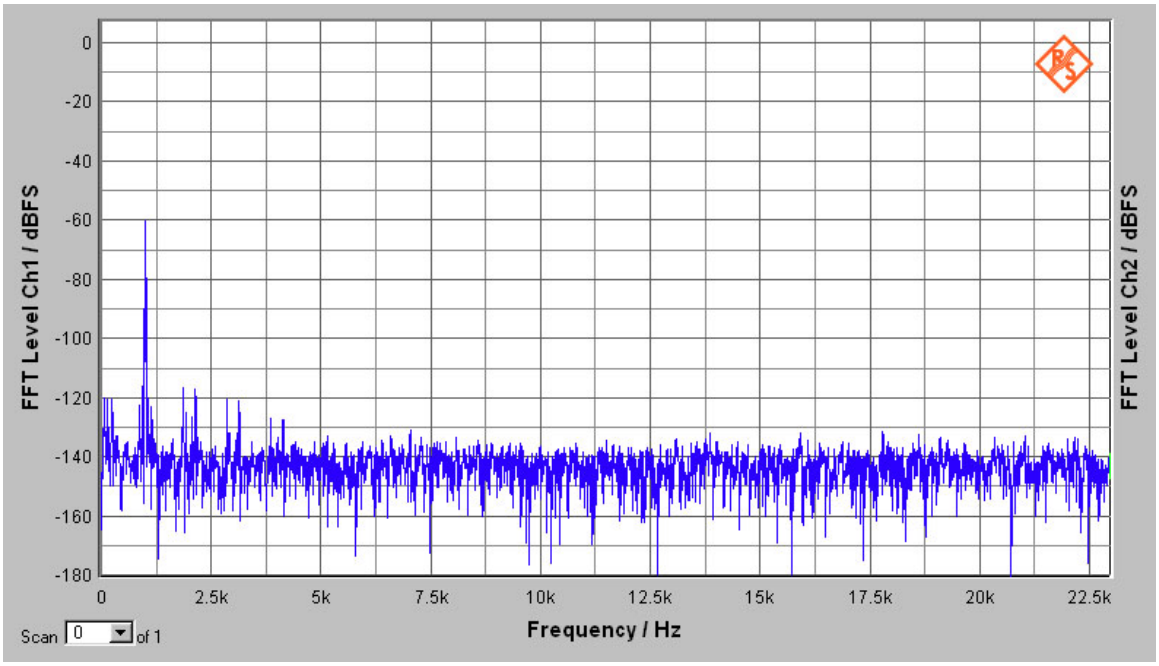


Figure 5. Output spectrum of the NTAD24 evaluation board for -60dBFS input signal and 48kHz sample rate.

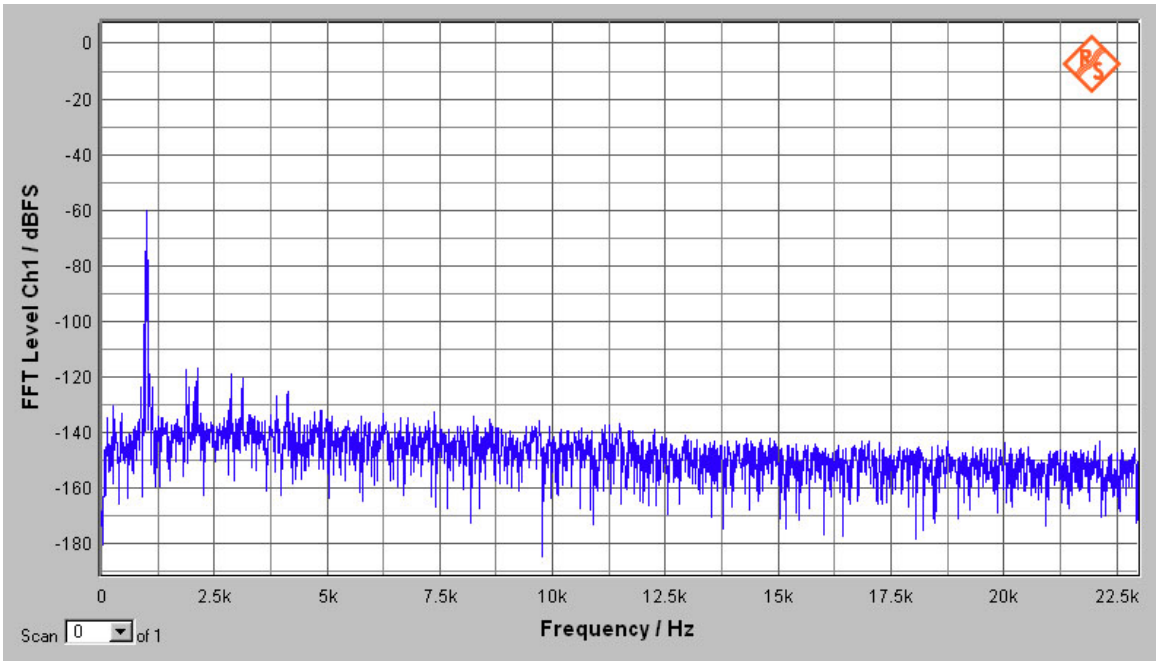


Figure 6. Output spectrum of the NTAD24 evaluation board for -60dBFS input signal and 48kHz sample rate (A-Weighted).

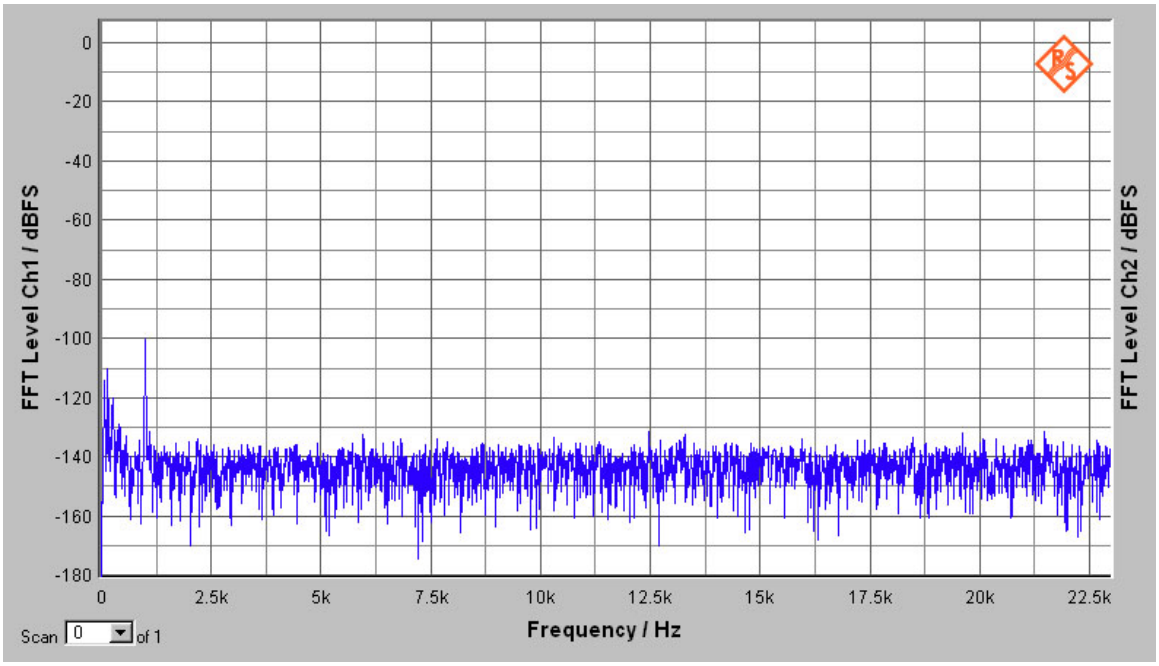


Figure 7. Output spectrum of the NTAD24 evaluation board for -100dBFS input signal and 48kHz sample rate.

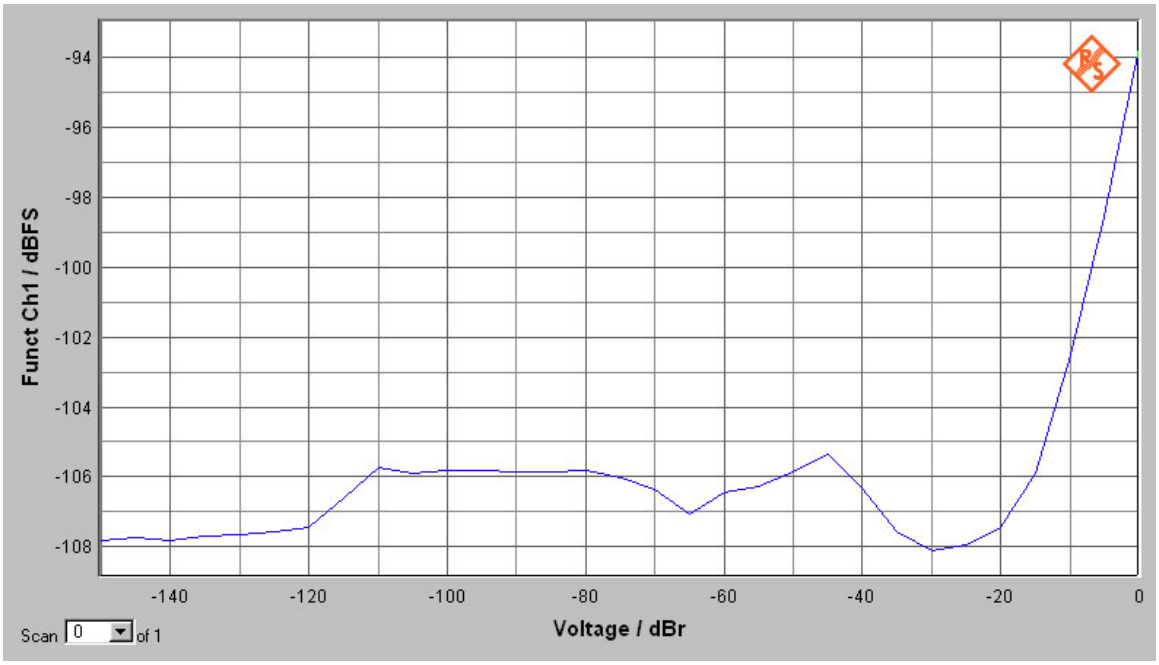


Figure 8. Noise level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 48kHz.

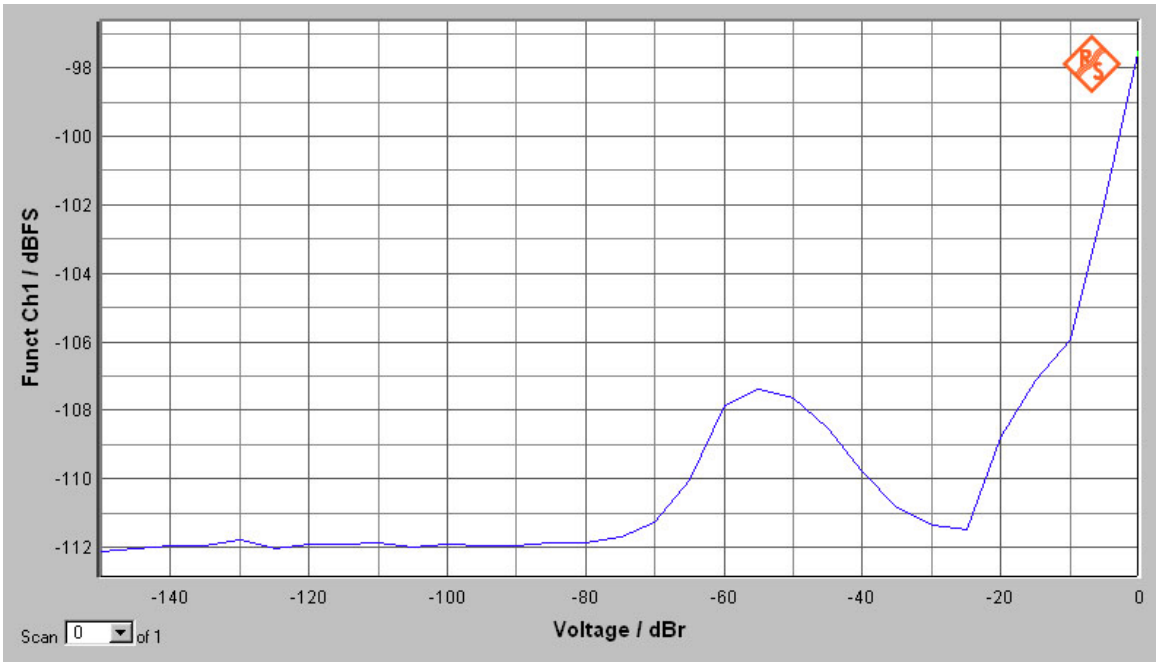


Figure 9. Noise level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 48kHz (A-Weighted).

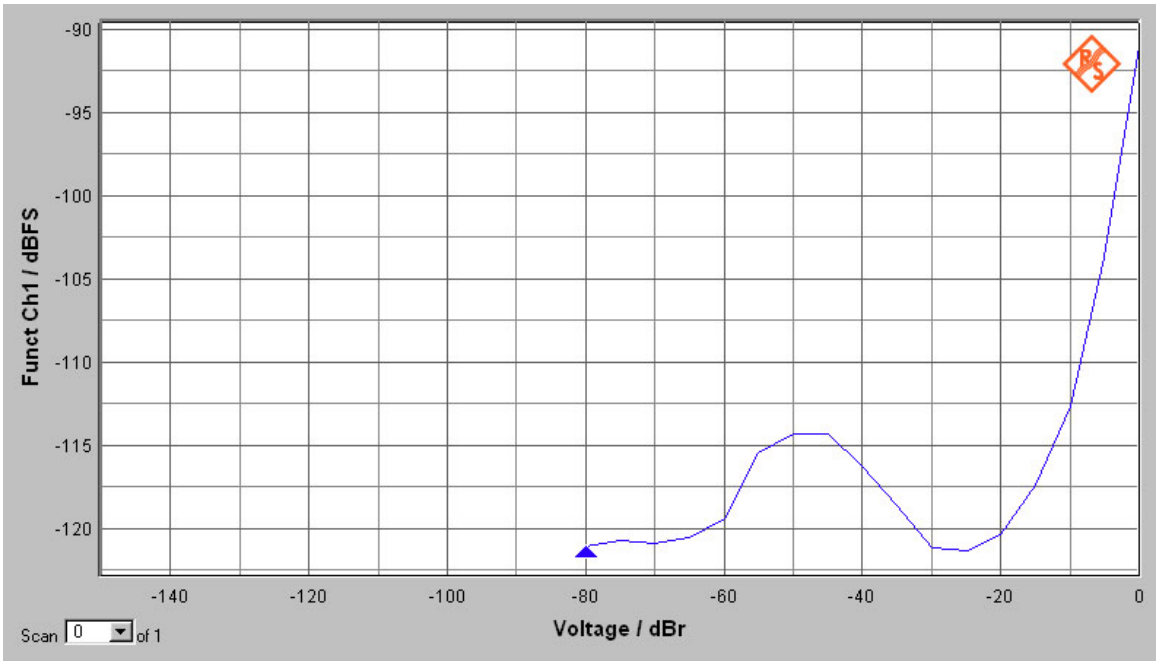


Figure 10. THD level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 48kHz.

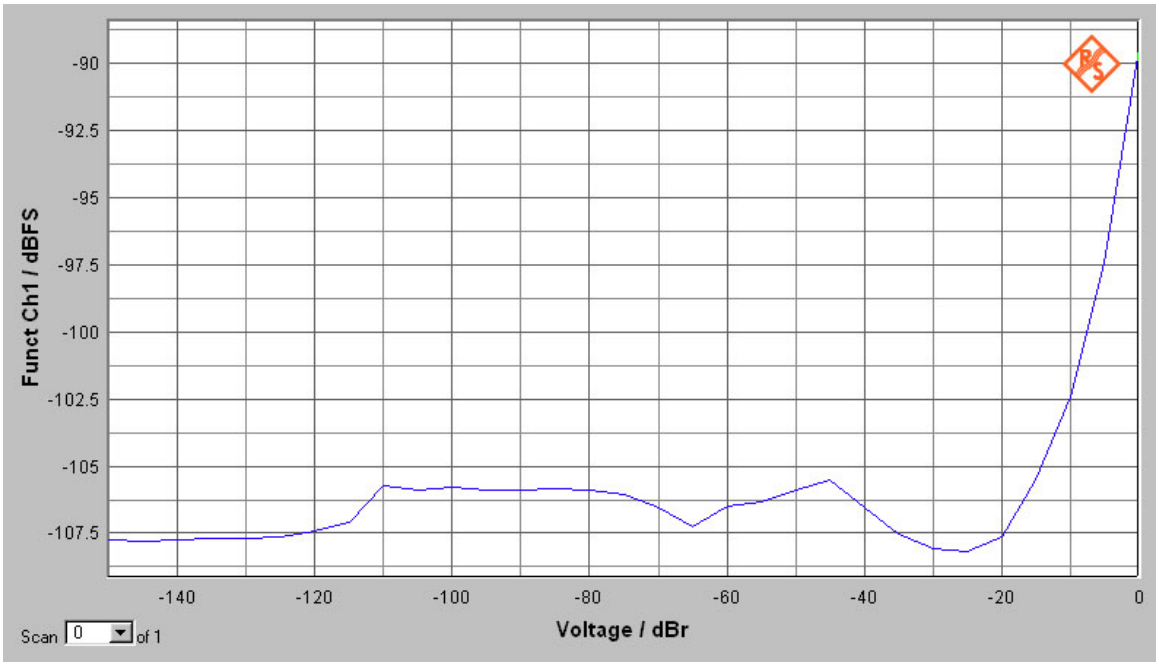


Figure 11. THD+Noise level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 48kHz.

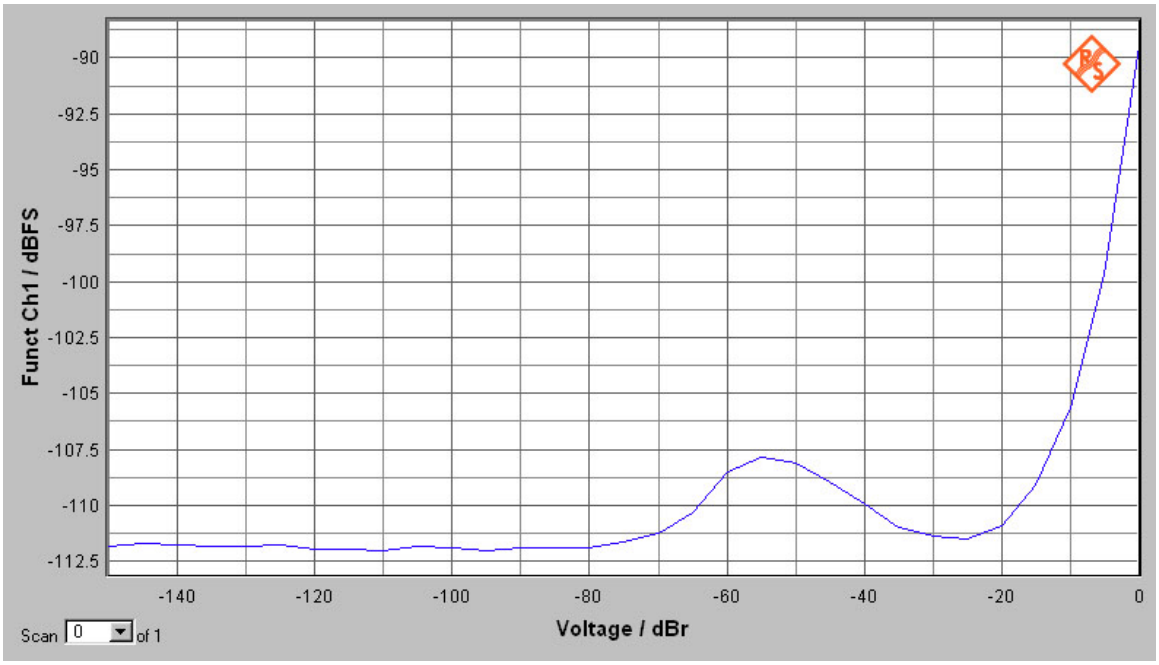


Figure 12. THD+Noise level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 48kHz (A-Weighted).

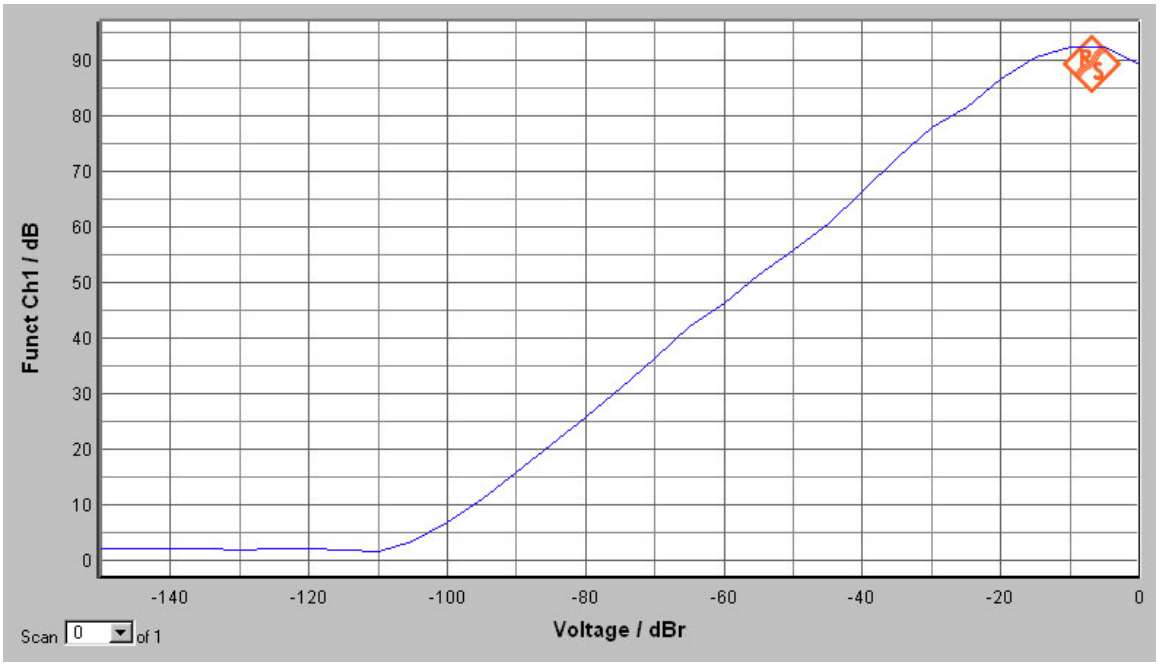


Figure 13. SNDR of the NTAD24 evaluation board versus the power of the input signal when sample rate is 48kHz.

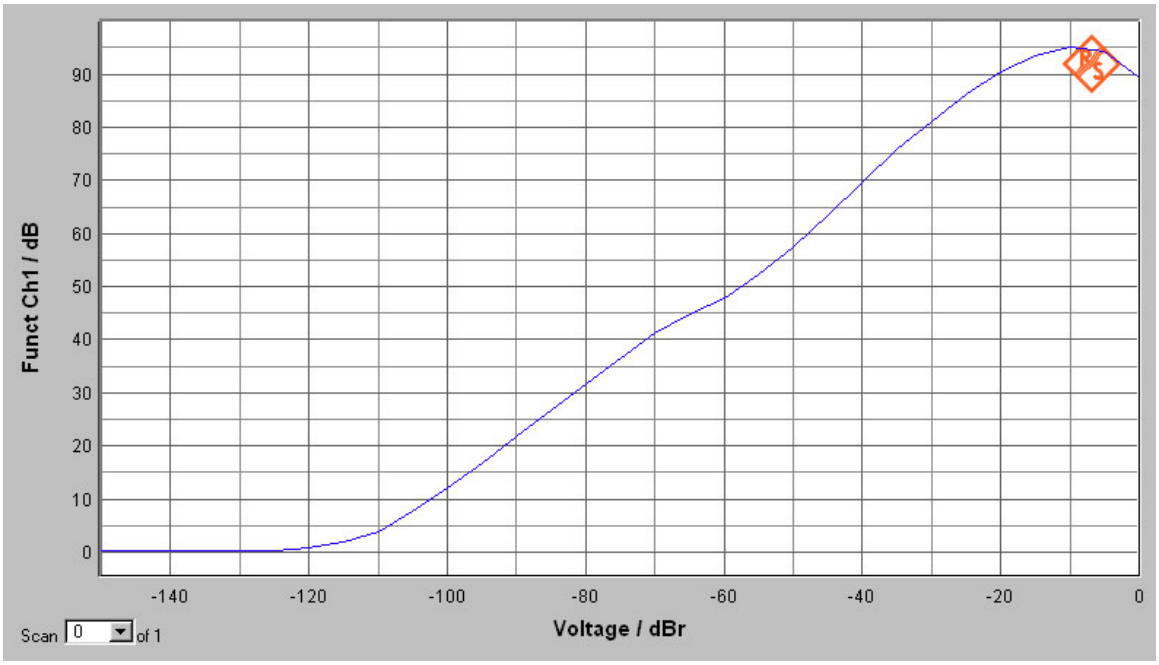


Figure 14. SNDR of the NTAD24 evaluation board versus the power of the input signal when sample rate is 48kHz (A-Weighted).

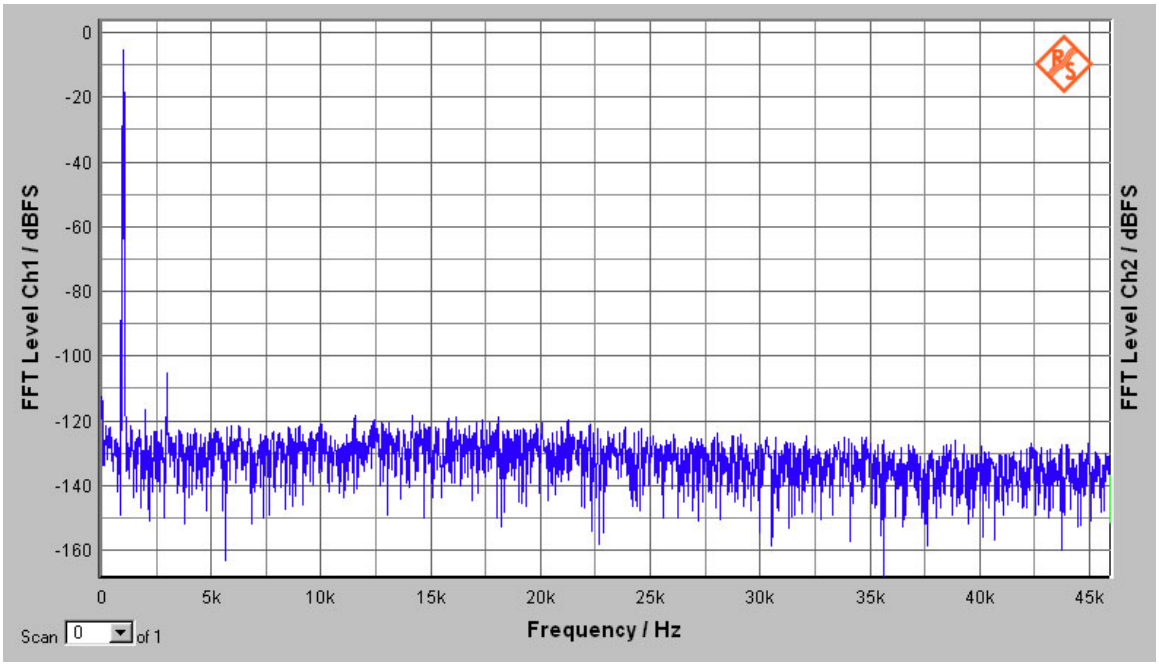


Figure 15. Output spectrum of the NTAD24 evaluation board for -4dBFS input signal and 96kHz sample rate.

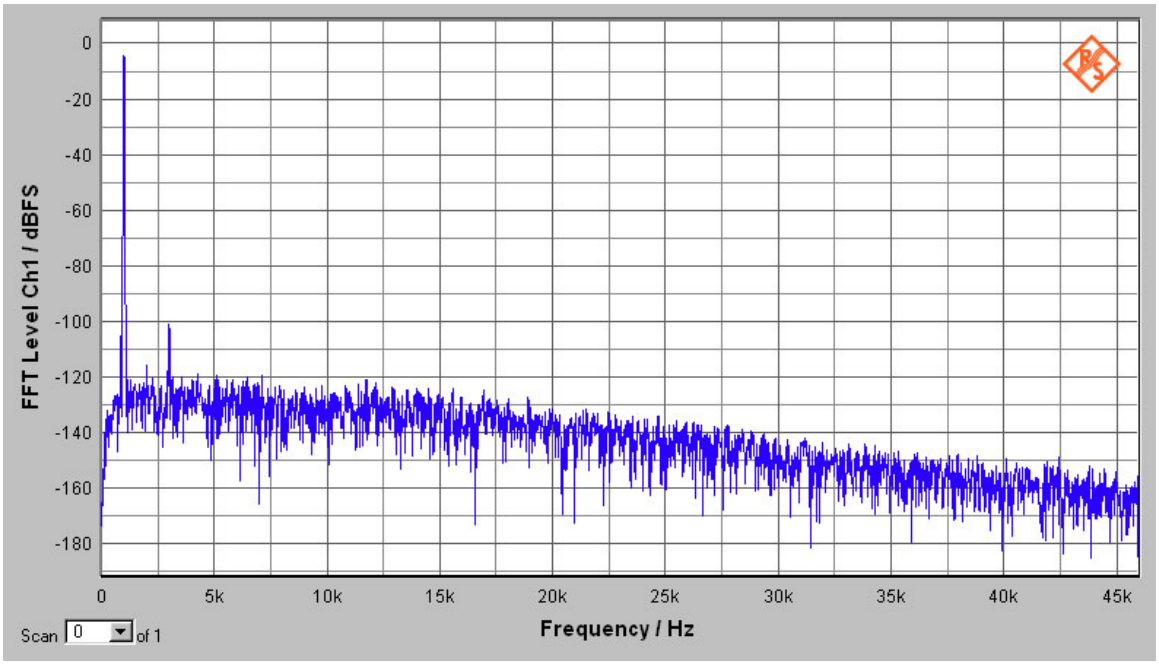


Figure 16. Output spectrum of the NTAD24 evaluation board for -4dBFS input signal and 96kHz sample rate (A-Weighted).

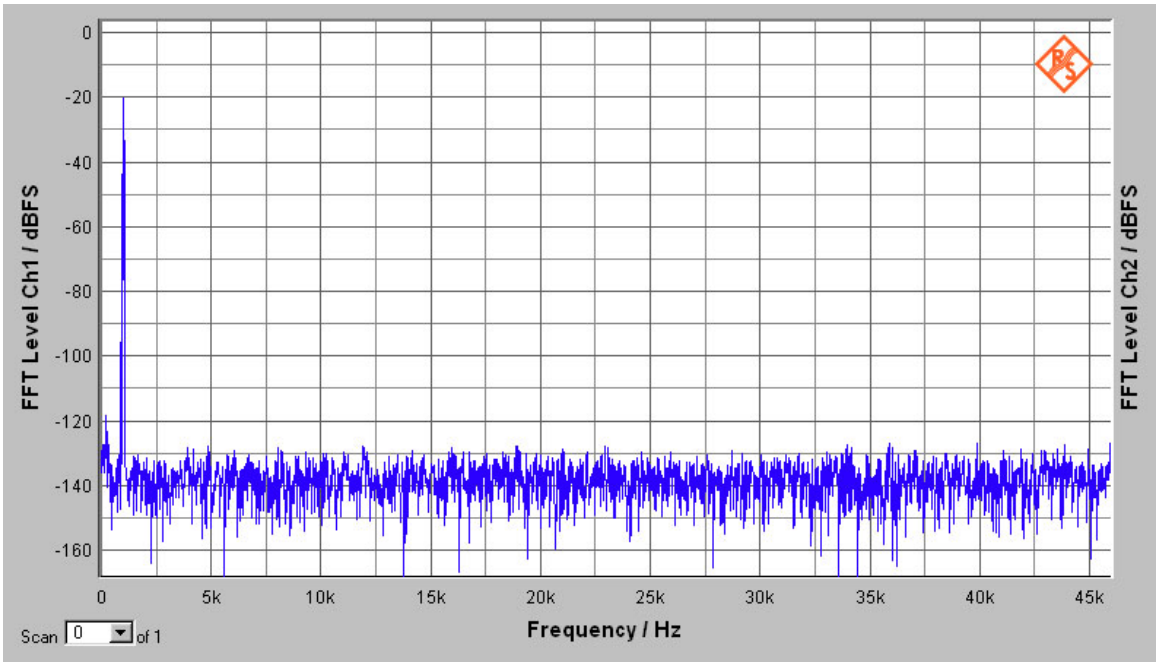


Figure 17. Output spectrum of the NTAD24 evaluation board for -20dBFS input signal and 96kHz sample rate.

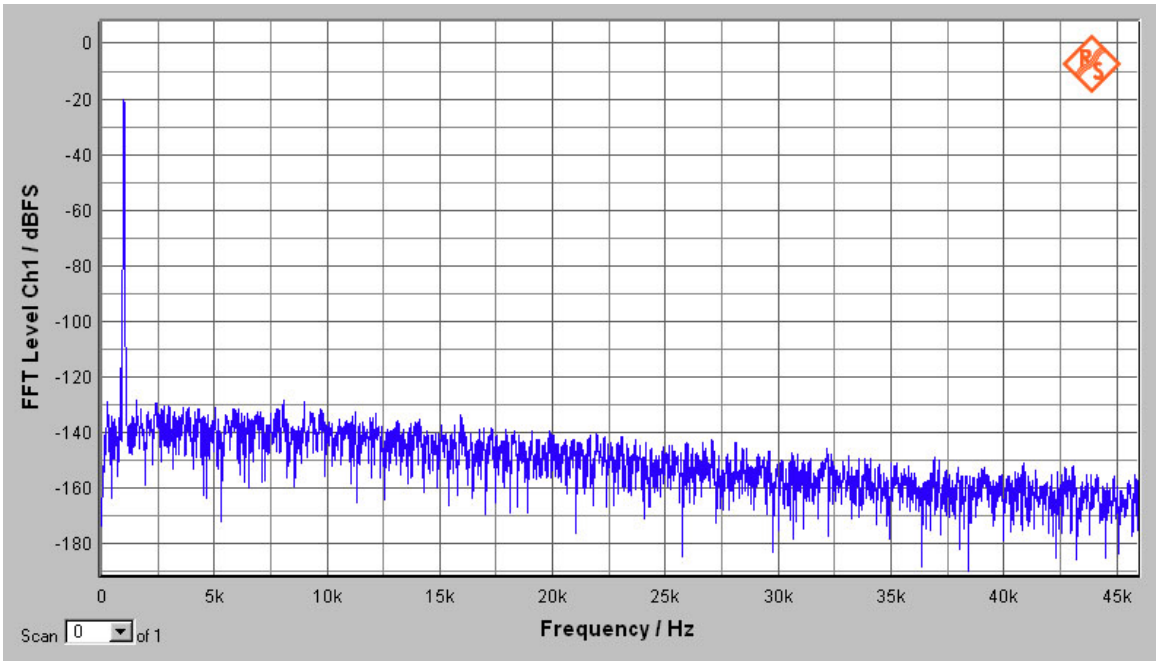


Figure 18. Output spectrum of the NTAD24 evaluation board for -20dBFS input signal and 96kHz sample rate (A-Weighted).

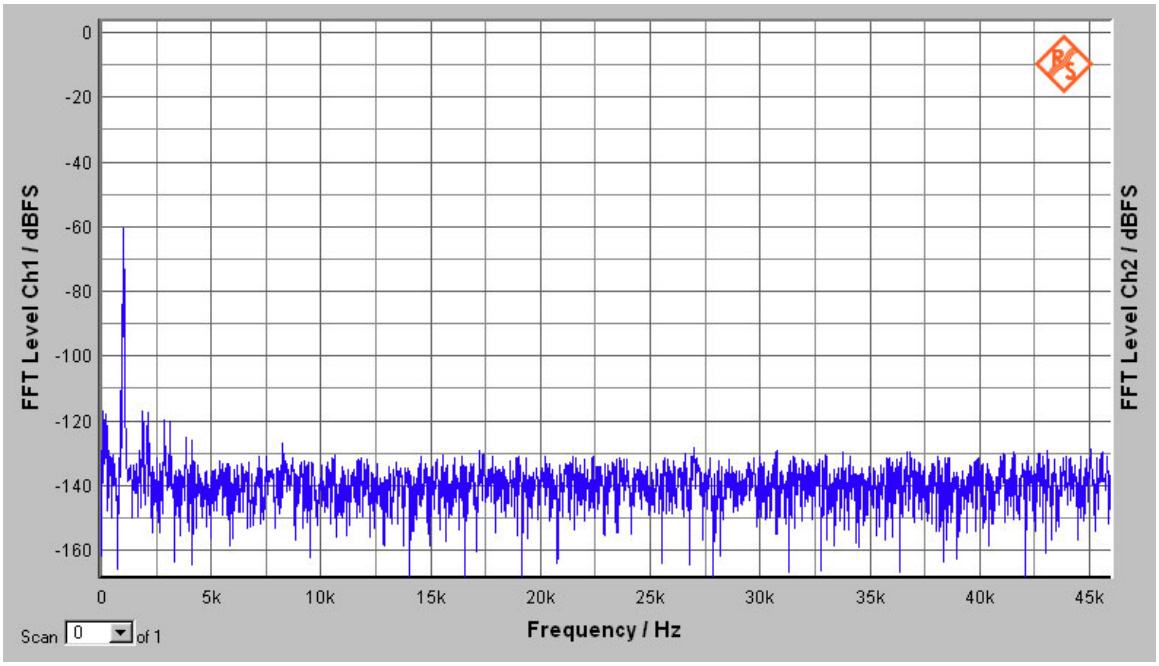


Figure 19. Output spectrum of the NTAD24 evaluation board for -60dBFS input signal and 96kHz sample rate.

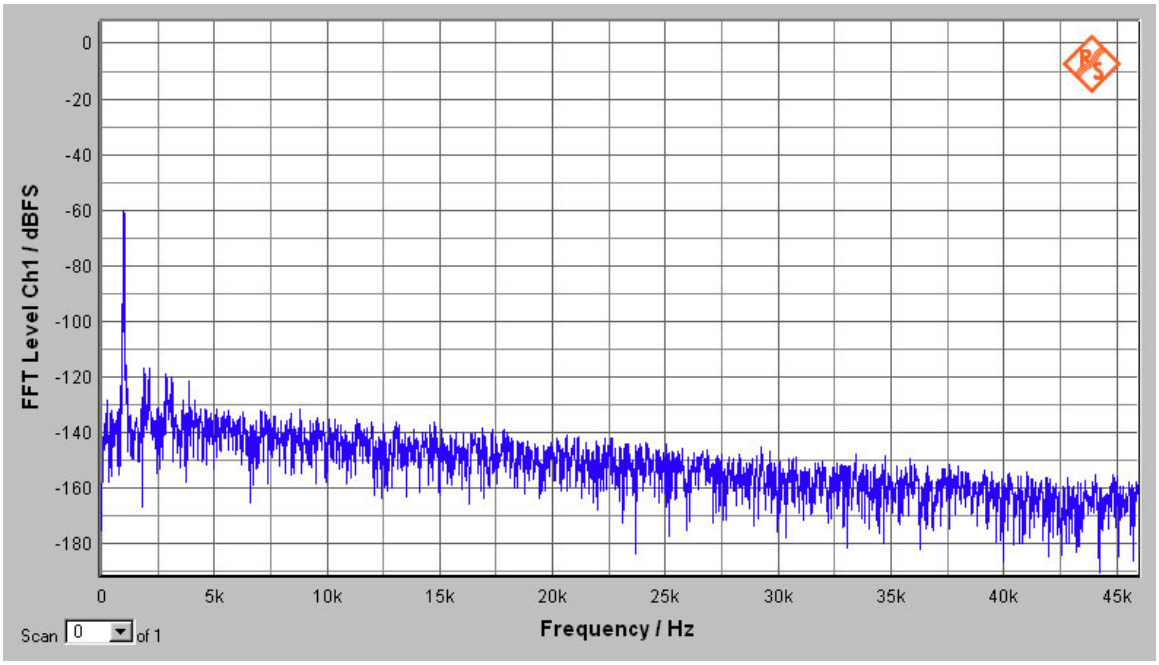


Figure 20. Output spectrum of the NTAD24 evaluation board for -60dBFS input signal and 96kHz sample rate (A-Weighted).

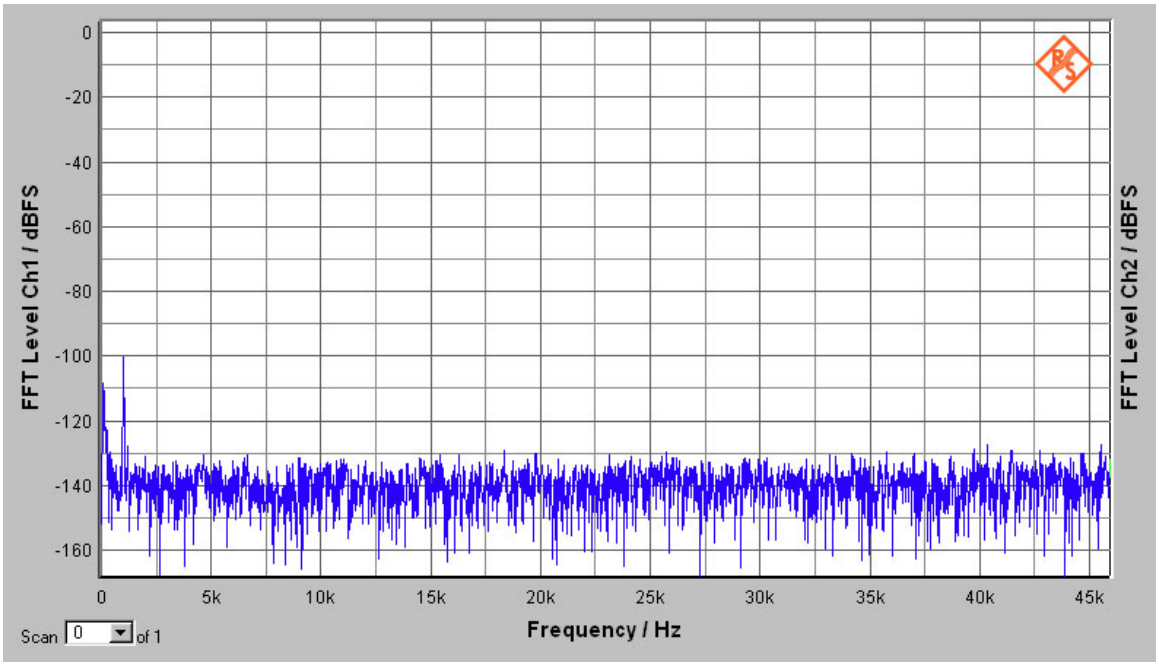


Figure 21. Output spectrum of the NTAD24 evaluation board for -100dBFS input signal and 96kHz sample rate.

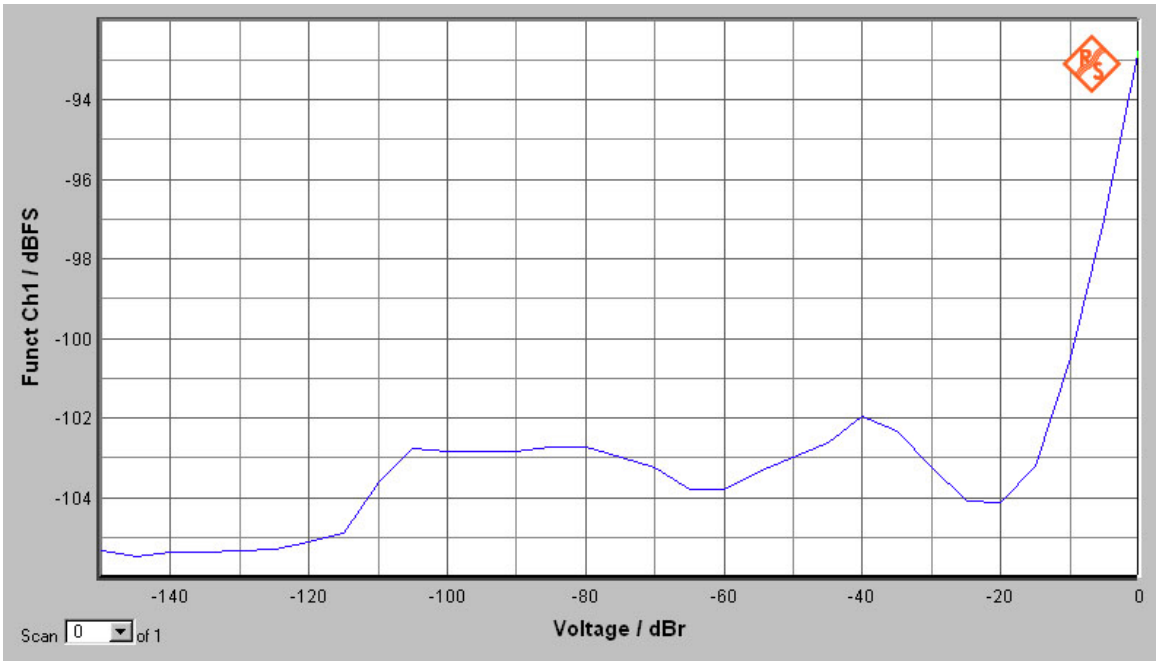


Figure 22. Noise level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 96kHz (BW=48kHz).

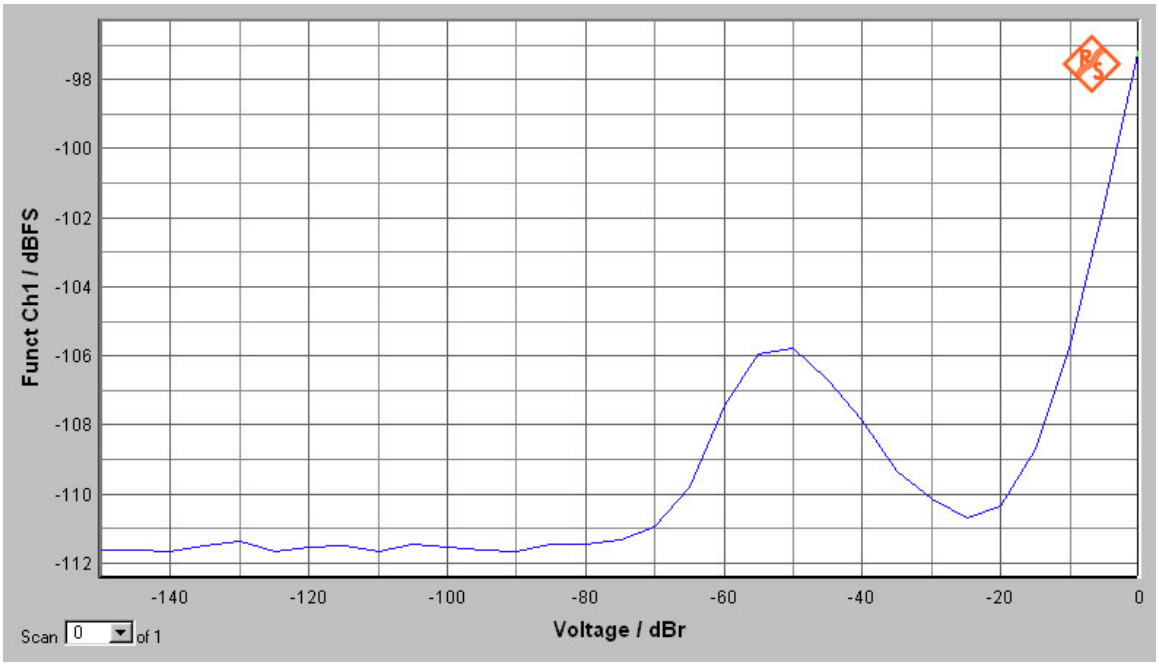


Figure 23. Noise level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 96kHz (A-Weighted, BW=48kHz).

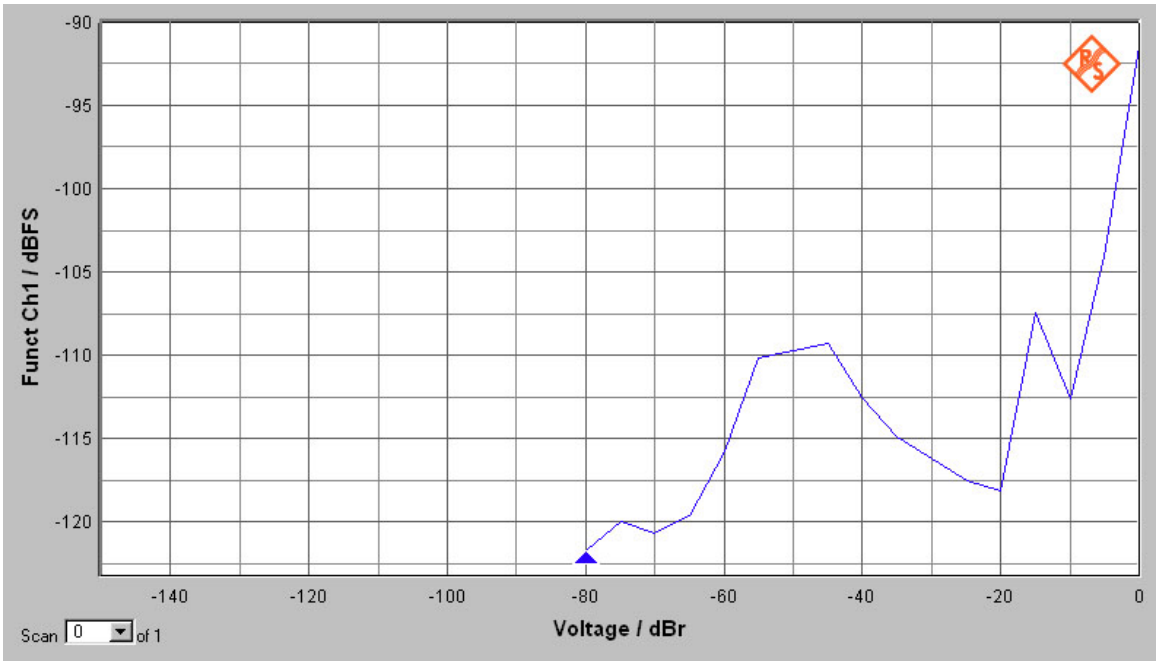


Figure 24. THD level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 96kHz (BW=48kHz).

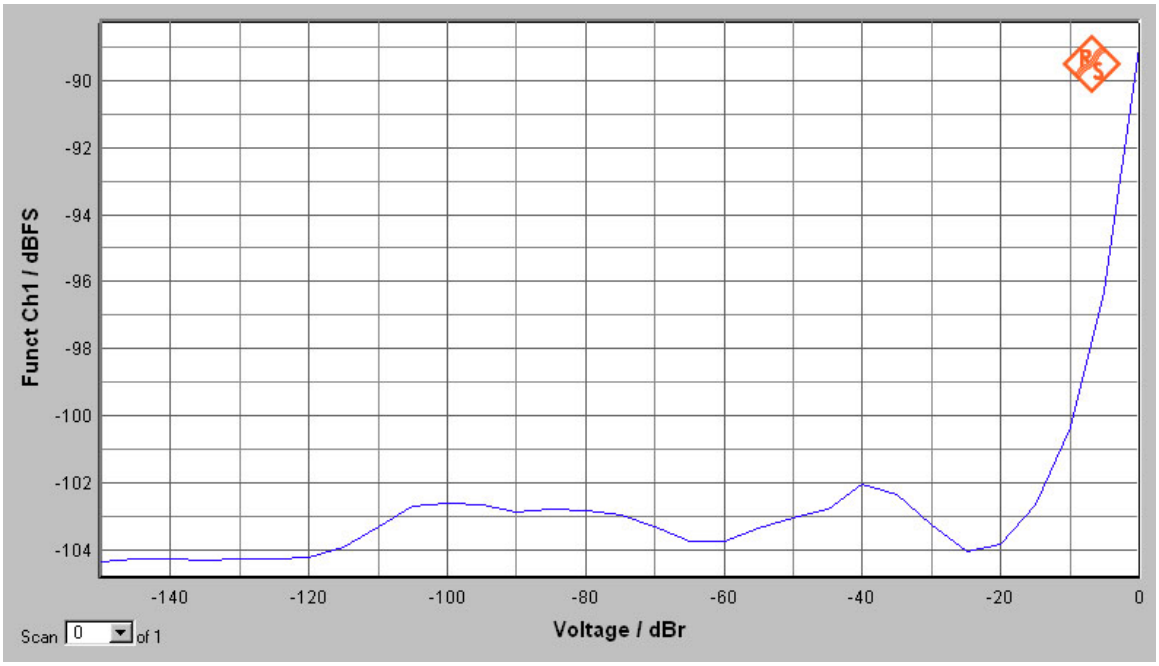


Figure 25. THD+Noise level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 96kHz (BW=48kHz).

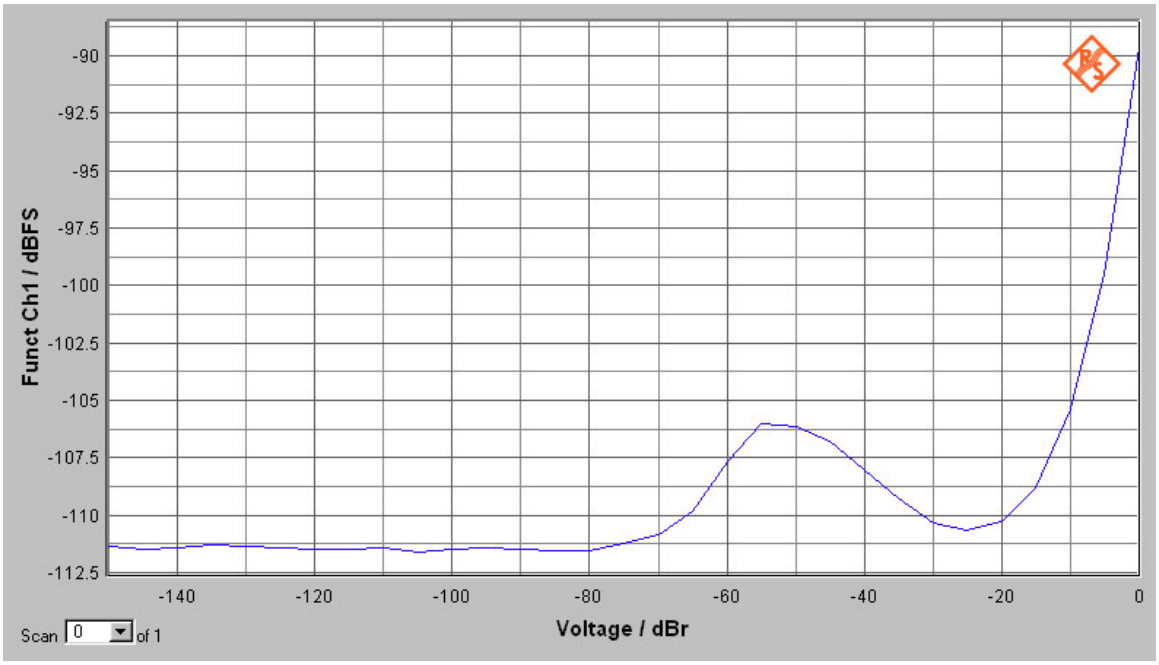


Figure 26. THD+Noise level of the NTAD24 evaluation board versus the power of the input signal when sample rate is 96kHz (A-Weighted, BW=48kHz).

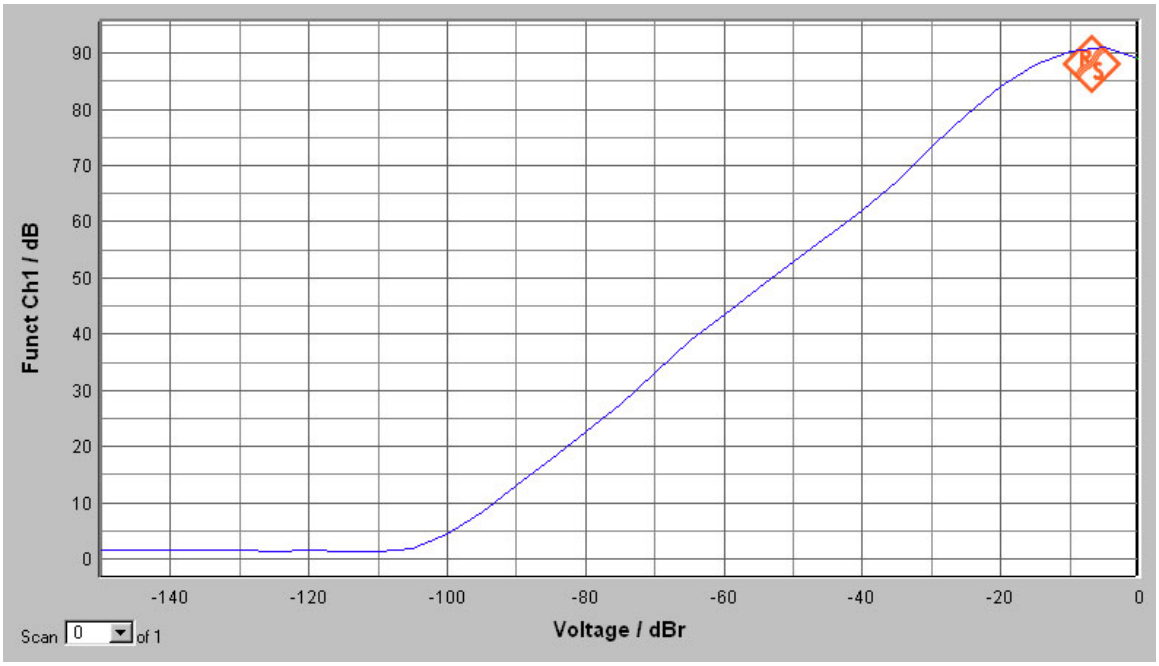


Figure 27. SNDR of the NTAD24 evaluation board versus the power of the input signal when sample rate is 96kHz (BW=48kHz).

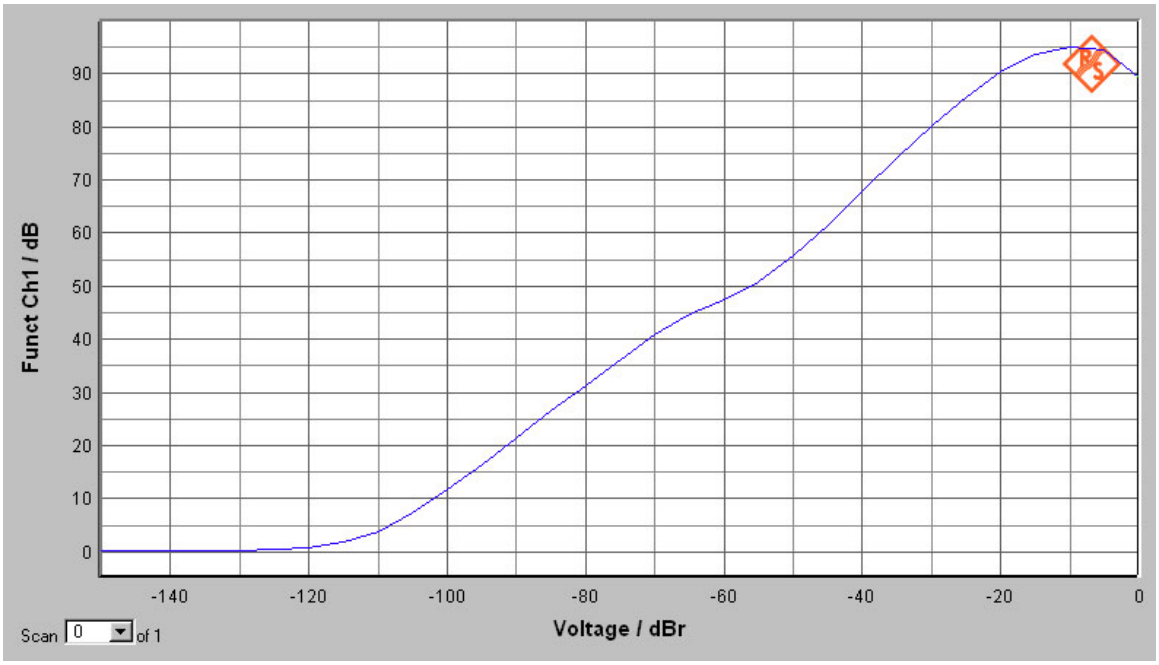


Figure 28. SNDR of the NTAD24 evaluation board versus the power of the input signal when sample rate is 96kHz (A-Weighted, BW=48kHz).

FUNCTIONAL DESCRIPTION

Device Architecture

The NTAD24 is a single channel mono ADC featuring multibit sigma-delta topology. The ADC is controlled by a bit-clock (SCLK) and synchronization signal called LRCLK.

General Overview

The NKDA24 is designed to run with an internal MCLK (MCLK) of 12.288 MHz and a modulator of 6.144 MHz. From this MCLK frequency, sample rates of 48 kHz, 96 kHz, and 192 kHz can be achieved on the channel. Pins M1 and M0 of the NTAD24 as well as Bits M1 and M0 of Control Register determine the sample rates (see Table 1). The internal clock should never be run at a higher frequency but may be reduced to achieve lower sampling rates. The modulator rate scales in proportion with the MCLK scaling.

OPERATING FEATURES

SPI Control Register Definitions

The NTAD24's Operating Mode is set by programming a Control Register via an SPI compatible port or via Pins. Table 3 details the format of the NTAD24's Control Word, which is 16 bits wide with 5 reserved Bits (Bits 10 to 15).

Serial Data Interface

The NTAD24's serial data interface consists of three pins (LRCLK, SCLK, SERIAL_OUTPUT). LRCLK is the framing signal for left and right channel samples and its frequency is equal to sampling frequency (f_s). SCLK is the serial clock used to clock the data samples from the NTAD24 and its frequency is equal to $64 \times f_s$ (giving 32 SCLK periods for each of the left and right channels). SERIAL_OUTPUT outputs the left and right channel sample data coincident with the falling edge of SCLK.

The serial data output supports all the popular audio interface standards, such as I^2S, left-justified (LJ), and right-justified (RJ). The Interface Mode is selected by Pins DF1-DF0 or programming the Bits DF1-DF0 of Control Register (see Table 2).

The data sample width can be selected from 16, 20, and 24 bits by programming Bits WW1-WW0 of Control Register (see Table 4).

I^2S Mode

In I^2S Mode, the data is left-justified, MSB first, with the MSB placed in the second SCLK period following the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the left channel data transfer, while a low-to-high transition on the LRCLK signifies the beginning of the right channel data transfer (see Figure 10)

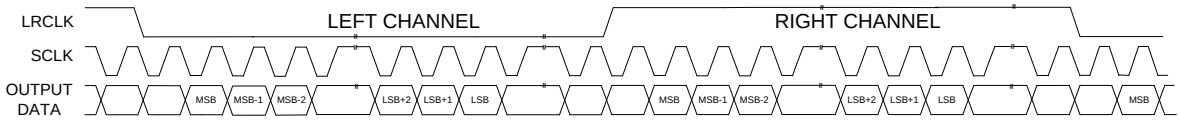


Figure TCP 7. I^2S Mode

Left-Justified Timing

In LJ Mode, the data is left-justified, MSB first, with the MSB placed in the first SCLK period following the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the right channel data transfer, while a low-to-high transition on the LRCLK signifies the beginning of the left channel data transfer (see Figure 11)

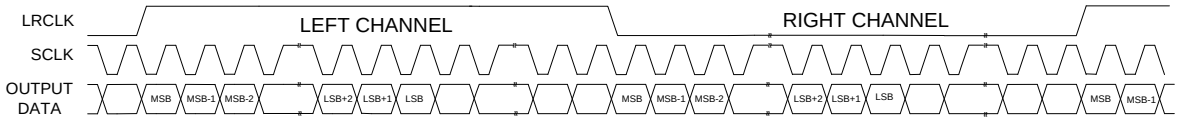


Figure TCP 8. LJ Mode

Right-Justified Timing

In RJ Mode, the data is right-justified, LSB last, with the LSB placed in the last SCLK period preceding the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the right channel data transfer, while a low-to-high transition on the LRCLK signifies the beginning of the left channel data transfer (see Figure 12)

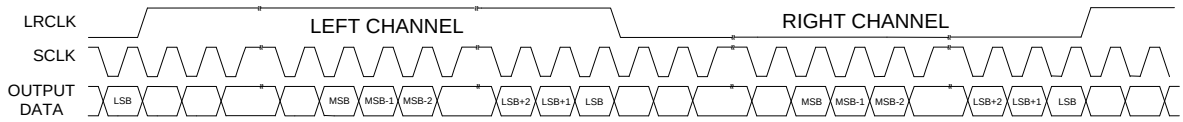


Figure TCP 9. RJ Mode

TEST METHOD & CONFIGURATIONS

General Description

The test is performed using the configuration setup shown in the following figure. In this configuration the NKDA24 EVB[1] is serving as a low frequency highly linear input signal generator for the NTAD24 EVB. The FPGA Board (Stratix II EP2S60 DSP Development Board) programs the NKDA24 EVB with a NikTek Semiconductor programming code. The digital output data from NTAD24 EVB is captured by means of the FPGA Board. The captured data is transferred to a PC and evaluated using NikTek Semiconductor analysis codes. It should be mentioned that programming of the FPGA Board and data logging is performed by Altera's Quartus® II software.

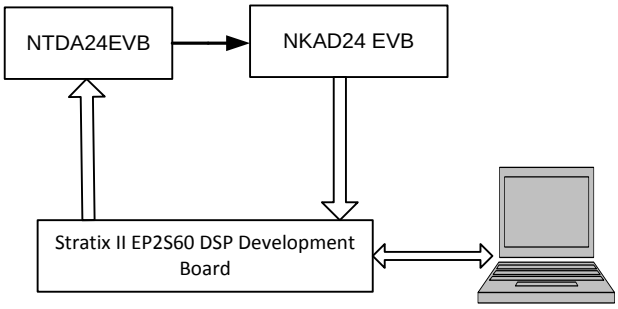


Figure S1. Test Configuration

List of Equipments

Type	Notes
NTAD24 Evaluation Board	The Main Board
Stratix II EP2S60 DSP Development Board	1) Programming the NTDA24 EVB 2) Capturing the NTAD24 EVB digital output data
NKDA24 Evaluation Board	Providing a low frequency, highly linear sinusoidal wave form (DC Test)
+5V & ±15V Rechargeable Batteries	Used as clean power supplies for NKDA24 EVB and NTAD12100 EVB
100Msps Oscilloscope + Multimeter a) 4-wire SMA Cable b) 4-wire SMA Cable c) XLR Cable	Checking the intermediate signals a) Connecting 4-pin headers from FPGA board to NKDA24 Evaluation board b) Connecting NTAD24 EVB to FPGA board c) Connecting NKDA24 EVB to NTAD24 EVB

[1] Evaluation Board

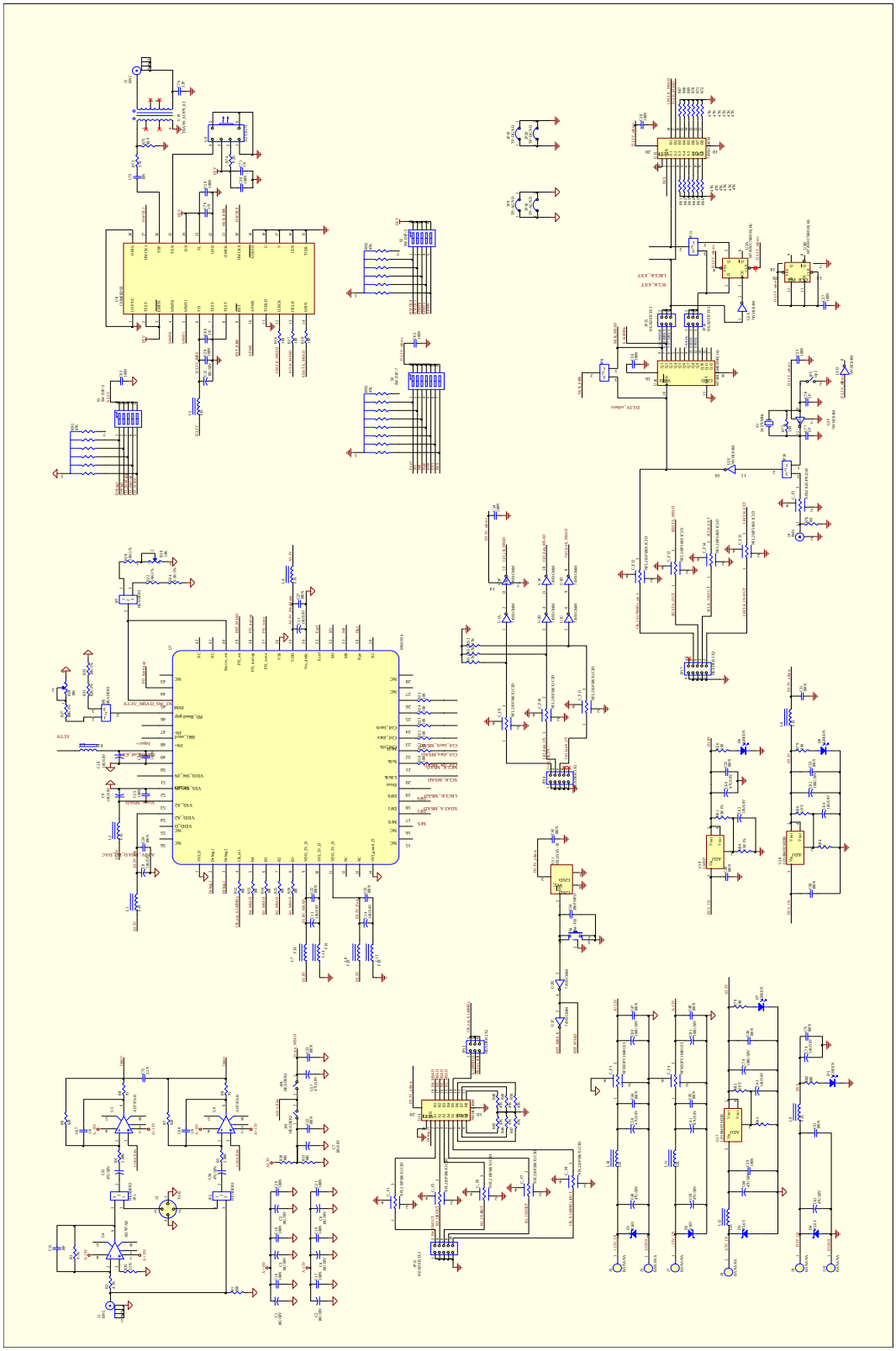


Figure S2. The Schematic of the evaluation board

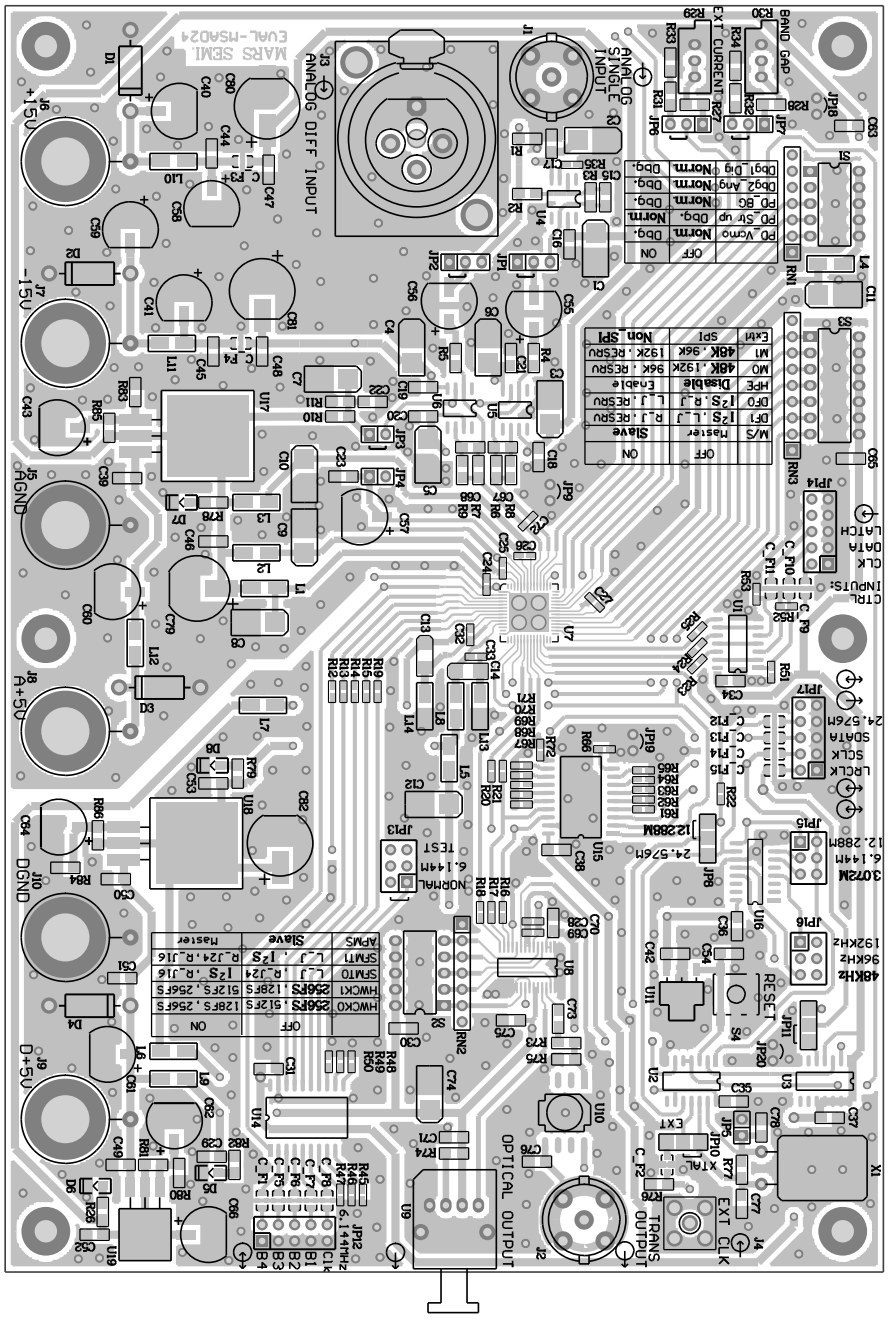


Fig. S3. Top layer of the PCB board.

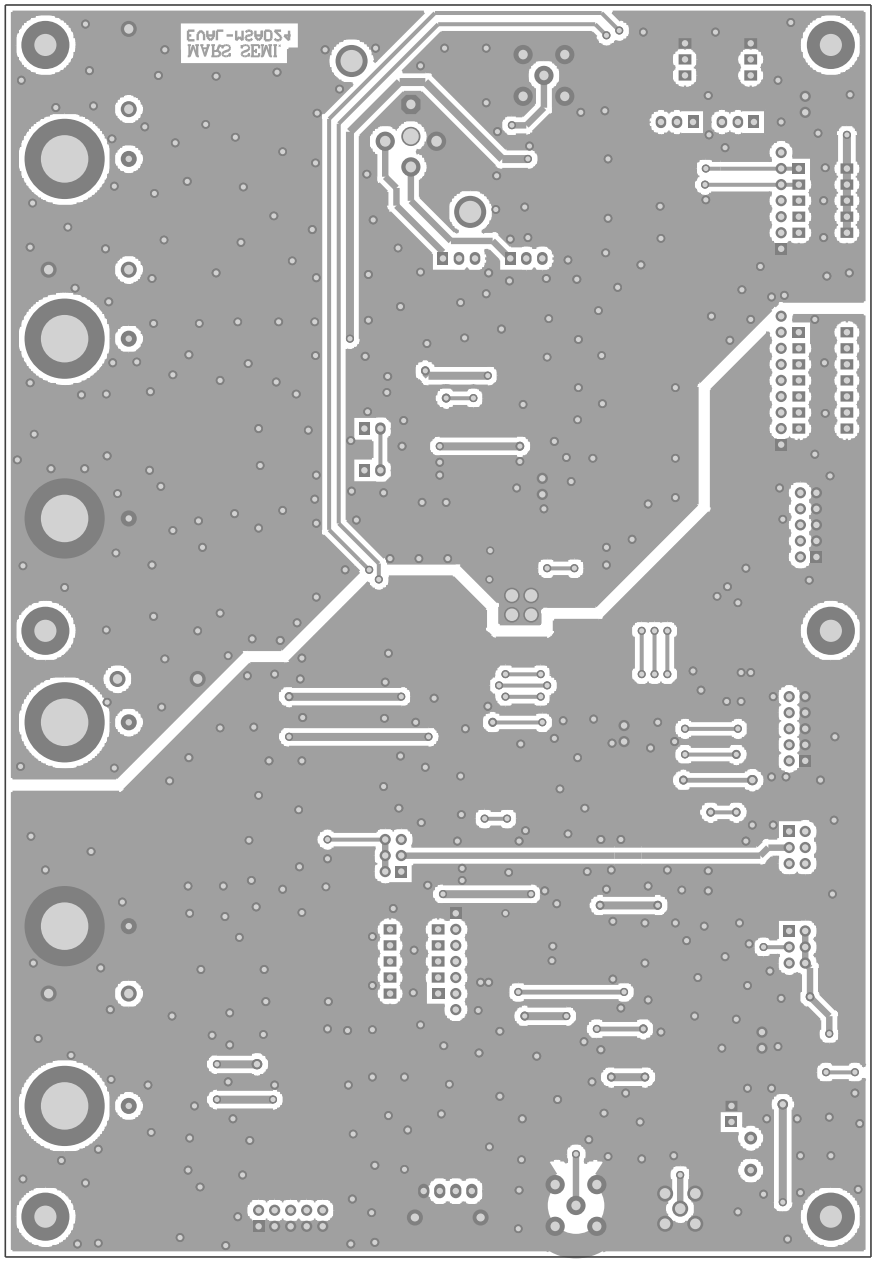
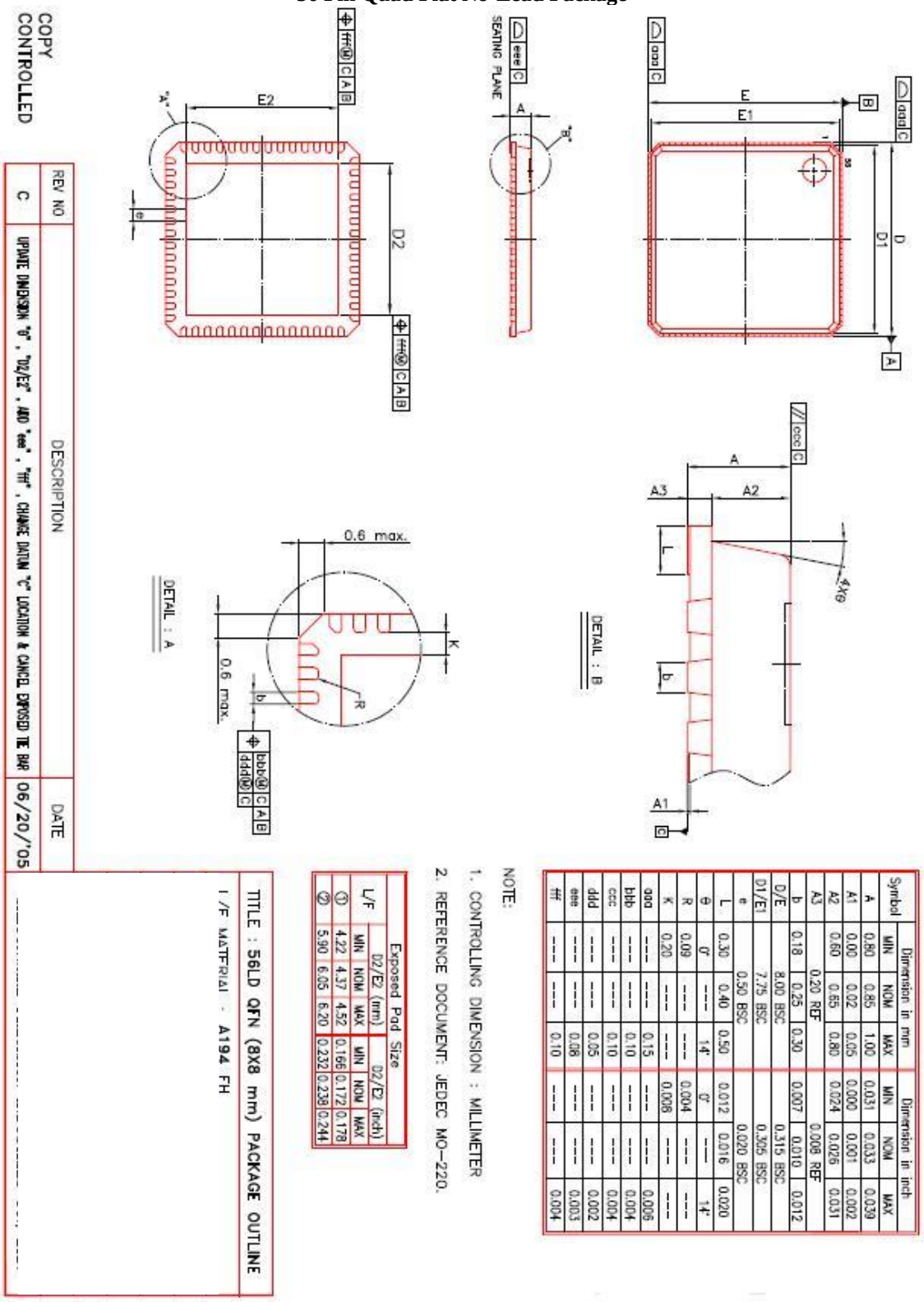


Fig. S4. Bottom layer of the PCB board.

OUTLINE DIMENSION
56 Pin Quad Flat No-Lead Package



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		8.00 BSC			0.315 BSC	
D1/E1		7.75 BSC			0.305 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	----	14°	0°	----	14°
R	0.09	----	----	0.004	----	----
K	0.20	----	----	0.008	----	----
aaa	----	----	0.15	----	----	0.006
bbb	----	----	0.10	----	----	0.004
ccc	----	----	0.10	----	----	0.004
ddd	----	----	0.05	----	----	0.002
eee	----	----	0.08	----	----	0.003
fff	----	----	0.10	----	----	0.004

	Exposed Pad Size					
	D2/E2 (mm)			D2/E2 (inch)		
L/F	MIN	NOM	MAX	MIN	NOM	MAX
①	4.22	4.37	4.52	0.166	0.172	0.178
②	5.90	6.05	6.20	0.232	0.238	0.244